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DARPA

ENABLING TECHNOLOGY FOR THIN FILM DISPLAYS

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This technical report has been reviewed and is approved for publication.

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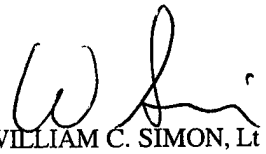

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13. ABSTRACT *(Maximum 200 words)*

This program has laid the foundations for rugged, flexible, bendable high performance thin-film transistor (TFT) backplanes for display and sensor/detector array applications and has further developed patterned organic layers for color OLED's using both wet and dry processes.

Innovations have been made in transistor materials and processing, substrate treatments and processing, and systems integration. Six backplane TFT technologies have been developed for flexible substrates:

(1) amorphous silicon TFTs on steel foils, which yields TFT structures which are rugged and dimensionally stable;
(2) polycrystalline silicon TFT complementary metal oxide on silicon (CMOS) on steel foils, which takes advantage of the high temperature tolerance of steel;
(3) high performance polycrystalline silicon (p-Si) TFT CMOS using a separation approach which allows full high-temperature processing and yields mobilities for holes and electrons over 300 square centimeters / volt-second;
(4) amorphous silicon (a-Si) TFTs on plastic (Kapton) foil using an amorphous silicon process optimized for 150°C,
(5) nanocrystalline silicon (n-Si) TFTs using processing that is adaptable to direct deposition on plastic foil substrates, and
(6) polymeric TFTs fully compatible with flexible substrates and demonstrating record mobilities.

In the OLED work, both wet and dry patterning for OLED processing have been found to be compatible with roll-roll processing and not to require vacuum. Wet processes (e.g. ink jet printing) have been found to depend critically on the final printed profiles which result from the drying process of the liquid. By developing a solvent-assisted diffusion process for organic molecules in polymers, which can temporarily depress glass transition temperatures by over 100°C, a practical large-area dry-patterning process has been developed for patterning color OLED's.

14. SUBJECT TERMS

Flexible displays, plastic and steel foil substrates, thin-film transistor (TFT), backplanes, complementary metal oxide semiconductor (CMOS), silicon TFTs, organic TFTs, ink-jet printing, organic light emitting diode (OLED), OLED patterning, roll-to-roll processing

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FOREWORD

This Grant F33615-98-1-5164 (ASTARS[1] WU[2] ARPHEC02; which was mistakenly referred to as HWIS[3] WU 71841105[4] on the 2nd and 3rd year funding Modifications P00001 and P00002) entitled "Enabling Technology for Thin Film Displays," was selected under Defense Advanced Research Projects Agency (DARPA) Broad Agency Announcement (BAA) 97-31, entitled "High Definition Systems (HDS)." This grant from the government to the Pennsylvania State University required the government to provide 100% of the total project funding of $1,907,670 under DARPA Order A940/xx(00),/57(99),/46(98) to Dr. Hopper at the Air Force Research Laboratory (AFRL) as DARPA Agent. Mr. Gurdial Saini of AFRL served as the contract monitor. Performance was over the period 17 August 1998 through 16 August 2001. Princeton University served as a subcontractor.

This report documents work enabled by earlier funding of the same research team:

(a) a grant F33615-94-1-1464 (ASTARS WU A9400105) to the Pennsylvania State University in the amount of $3,269,482 for performance during the period June 1994 to September 1997, which produced the interim technical report AFRL-HE-WP-TR-1999-0164 entitled "Strategic Intent: Establishment of a U.S. Display Technology Infrastructure Through the Funding of Shared Research Resources" and

(b) a task via the AFRL In-House Support contract F33601-93-D-J019 (UNC Lear Services) Purchase Order A66610-000 for $242,500, for performance during the period 1 July-31 December 1997, which produced a final technical report AFRL-HE-WP-TR-1999-0189 entitled "Backplane Arrays on Flexible Substrates."

This report has been formatted in accordance with a commercial standard, with tailoring from the AFRL Scientific Technical Information Office. That standard is:
"Scientific and Technical Reports—Elements, Organization, and Design,"
American National Standard ANSI/NISO Z39.18-1995 (NISO Press, Bethesda MD, 1995),
which is available electronically via the following website address:
http://www.wrs.afrl.af.mil/library/sti-pubh.htm

The technical review of this document was accomplished by Dr. Hopper and Mr. Saini of AFRL.

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[1] A Science and Technology Activity Reporting System (ASTARS)
[2] Workunit (WU)
[3] Human Effectiveness Directorate Workunit Information System (HWIS)
[4] HWIS WU 71841105 is, in fact, the HWIS WU renumbering assigned to in-house ASTARS WU 20030664.

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1. SUMMARY

This program had tasks that laid the foundations for rugged, flexible high performance thin film transistor (TFT) back planes for display and sensor/detector array applications. The program also further developed patterned organic layer technology for color organic light emitting diode (OLED) displays.

Task 1 addressed the questions of (1) how high performance TFTs can be attained on lightweight plastic and (2) how integrated systems with TFT backplanes and sensors, detectors, and/or displays can be attained on plastics. The first question of how to enable high performance poly-Si TFTs on plastics was approached by both direct deposition on plastic and separation/application-onto-plastic methodologies. In the direct deposition approach, microcrystalline silicon TFTs fabricated with processing flows compatible with many plastics were attained. In the separation approach, several separation technologies (deposited sacrificial layers and self-assembled sacrificial layers) were explored. This separation approach allows TFTs to be fabricated on "mother" substrates, then to be separated, and then to be applied to plastic laminates. The separation approach opens the door to the use of high temperature processing while constructing the TFTs on the "mother" substrate and thus opens the door to true high performance TFTs. We made such transistors, both n and p-channel, for this separation approach.

In Task 1, we also demonstrated that complex integrated systems could be formed on lightweight plastics. As examples, we showed how laser desorption mass spectroscopy structures and gas sensors can all be achieved on plastic. We also demonstrated fuel cell structures for powering integrated systems on plastic.

In this Task 1 we also greatly expanded the boundaries of flexible, silicon based thin film transistors made on substrates of plastic or steel foil for active matrix display backplanes. The goals of this portion of Task 1 were stated as follows. "Metal foil substrates and planarization techniques will be identified that enable the bending of TFTs and OLEDs made on these substrates to a 1-mm radius of curvature. A multilayer vapor barrier on transparent plastic will be used as the substrate for OLEDs and will be shown to have degradation as low as that of OLEDs made on glass."

In the preparation and use of substrate foils we went considerably beyond our goal, in response to growing industrial interest in guidance on flexible TFT backplanes. On the other hand, we did not pursue the development of a vapor barrier, because during the grant period that goal became a central project of OLED manufacturers.

We further developed our 150°C technology for making a-Si TFT on Kapton E substrate foils. These TFTs perform similarly to a-Si TFTs made in the conventional temperature range of 250°C to 300°C on glass. We introduced a new polycrystalline silicon TFT technology on steel foil substrates. Because this materials technology can be processed at temperatures of at least 950°C, it opens the door to CMOS circuits made by rapid processes on a flexible substrate. We demonstrated such CMOS circuits. We also

introduced nanocrystalline silicon as a TFT material for both p and n channel devices, and demonstrated a CMOS inverter made on glass substrate at 320°C. Toward the end of the grant we showed that p and n channels can be made in nanocrystalline silicon at 150°C. This demonstration made nc-Si a candidate for a CMOS technology on plastic substrates. Thus we have added two silicon based CMOS capable options for the fabrication of flexible TFT backplanes.

We also put the interaction of mechanical stress and electrical performance of amorphous silicon TFTs on a quantitative experimental and theoretical footing. We showed that a-Si TFTs can be strained uniaxially by approximately 0.5% in tension, and by at least 2% in compression before they fail electrically, by mechanical fracture. These strain values can translate to radii of curvature of 1-mm and even less, if certain geometries and TFT/substrate combinations are used. Sub-fracture strain has a minor effect on electron field effect mobility, which increases in tension and decreases in compression at a rate of 25% of mobility per 1% of strain. Releasing the strain restores the TFT's initial electrical characteristics. This work has initiated a quantitative approach to the proofing of TFT backplanes and other thin film electronics against mechanical stress.

Two of our a-Si TFT on foil technologies were adopted by companies.

Task 2 focused on electronic materials printing for low cost display elements. The goal of this work has been to develop printing-based methods for the production of high-efficiency displays based on organic light emitting diodes (OLED's) over large area. Printing based methods are more attractive for high volume roll-to-roll manufacturing than conventional microfabrication techniques such as photolithography and etching. In this work, printing techniques are investigated to pattern the organic layers so that pixels which directly emit red, green, and blue light can be formed for realizing color in a high-efficiency approach. These printing techniques include ink-jet printing and a patterned dry transfer process. Ink jet printing has the advantage of being conceptually simple, but is greatly complicated by requirements for the organic materials being printable and by droplet drying dynamics. Patterned dry transfer approaches are very promising, especially when combined with approaches to lower the glass transition temperature. Both methods have been used to integrate three-color devices.

In Task 2 we also addressed the problem that most of the light generated in traditional OLED's is trapped in the substrate (and thus wasted) because of total internal reflection due to the high index of refraction of the substrate. Because a potential showstopper problem for OLED displays is their temperature rise caused by power dissipation, such waste of photons is not acceptable. Therefore, we developed the most efficient methods to increase the output coupling of light, and developed approaches for implementing such methods which are compatible with roll-to-roll manufacturing, such as lamination. Fundamental modeling was carried out to determine how much light is actually trapped in the substrate, and to show that a ~3X increase in efficiency is possible with substrate.

Task 3 focused on the invention of organic thin film transistors (OTFTs), which can be deposited and processed at low temperatures. The OTFT performance now rivals or exceeds that of silicon inorganic thin film transistors (ITFTs) fabricated from the current industry standard material, inorganic amorphous silicon infused with hydrogen (a-Si:H). The low process temperatures required for OTFTs (150 °C), as compared to silicon ITFTs (typically 350 °C for a-Si), allow fabrication on a range of surfaces including cloth, paper, or polymeric substrates. Pentacene-based TFTs on flexible, low-temperature polymeric substrates with good performance characteristics were fabricated: field-effect mobility > 1 cm^2/V-s, on/off current ratio > 10^8, and threshold voltage near zero were obtained. These TFT characteristics are comparable to those fabricated from a-Si. Using these devices, digital and analog circuits were fabricated with active matrix display pixel array, and integrated OTFT - organic light emitting diode active pixels. These results demonstrate OTFT utility for a variety of low-cost or large-area electronics applications.

Appendix A documents intellectual property created with support from this DARPA-funded, AFRL-managed research grant in the form of patents.

Appendix B lists publications and presentations that report research accomplished under this grant in much greater detail than in this technical report. Inclusion of this list enables this report to be much shorter and avoids unnecessary duplicative reporting of massive research results.

Appendix C identifies degrees granted (doctoral, masters) or experience provided (postdoctoral research associates, graduate and undergraduate research assistants) to personnel who were supported by this grant while members of the research groups led by the authors of this report. The current positions (in industry or academia) held by persons trained under this program are also noted.

2. INTRODUCTION

This effort concentrated on root causes hindering thin film displays. Research was conducted in three inter-related areas: (1) novel substrates and encapsulation, (2) electronic materials printing to enable low cost fabrication of display elements (TFTs and OLEDs), and (3) organic TFTs. The objectives and goals as stated in the SoW (see Grant F33615-98-1-5164, Attachment 1) were as follows:

Statement of Work (SoW)

"Enabling Technology for Thin Film Displays"

Task 1: Novel Substrates and Encapsulation

The recipient shall explore the capabilities of metal foil substrate for flat panel displays, in particular, active matrices, and will develop a transparent multilayer barrier against water and oxygen permeation. Foils of strong and tough metals, like steel and Metglass, with thickness down to at least ½ mil (12.5 mm) will be explored for their ability to support TFTs and OLEDs when bent to small radii. Techniques for foil planarization and passivation shall be developed. The goal is to demonstrate functioning devices at a bending radius of 1 millimeter. A novel concept for a vapor and oxygen barrier is introduced in the form of a multiplayer inorganic/organic composite coating. This coating will be made of SiO2 or SiN/polyimide multilayers, and is designed to combine the good barrier properties of inorganic layers with long diffusion paths through the polyimide.

Task 2: Electronic Materials Printing for Low Cost Display Elements (TFTs and OLED's)

The lithography and etching steps for display elements, which dominate cost and throughput time, will be replaced by the direct patterned printing. In principle, it should be possible to fabricate entire circuits and displays by a sequential series of printing machines, which we will demonstrate by all printed TFT's, OLED's, and ring oscillators at the end of three years. Furthermore, to provide a process which is flexible and reconfigurable for small lot military products, the research team will develop printing processes which are directly controllable from computer databases, such as laser printing and inkjet printing (as opposed to screen printing). Direct patterned printing will also make it possible to fabricate patterned structures using materials not amenable to wet photolithographic patterning, such as organic materials.

Task 3: Organic TFTs

The recipient shall develop high-performance, manufacturable organic thin film transistors (OTFTs) for use in thin film displays. Such devices will allow manufacturing on polymeric substrates which will result in rugged, lightweight, lower cost and perhaps flexible displays. During earlier research, OTFT materials and processing techniques that resulted in world records for organic transistor field-effect mobility, current on/off ratio, and subthreshold slope were developed. The research team will build on this foundation to develop a manufacturable OTFT process and to develop OTFTs on plastic substrates. The focus of effort will be on pentacene-based devices but will also explore alternative materials that may offer even higher performance of enhanced manufacturability. The research team will also develop plans to collaborate with Princeton to integrate OTFTs and organic light emitting devices (OLEDs) and to develop low cost printable circuit materials.

The research accomplished to address Task 1, Task 2, and Task 3 is documented in sections 3.1, 3.2 and 3.3, respectively.

3. METHODOLOGY, RESULTS, AND DISCUSSION

References are numbered separately for sections 3.1.1, 3.1.2, 3.2.1, 3.2.1, 3.2.2, 3.2.3, and 3.3.

3.1 Novel Substrates and Encapsulation--Grant Task 1 -- Fonash and Wagner Groups

3.1.1 Enabling Technologies for High Performance Poly-Si TFTs and Systems on Plastic—Grant Task 1—Fonash Group (Penn State)

Details of work summarized in this section has been reported in the literature [1-22].

3.1.1.1 Direct Deposition onto Plastic--Micro-crystalline Si TFTs: Introduction and Methodology

One approach we pursued to fabricate high performance Si TFTs on plastic substrates was to use direct deposition. Our approach was based on use of a high density plasma (HDP) source since such sources offer unique chemistry reaction paths. This work proved highly successful and all processing temperatures used were less than or equal to 340 °C. The silicon films in this work were all microcrystalline and to demonstrate our approach we used these films to build N-channel microcrystalline silicon (mc-Si) thin film transistors (TFTs) on glass. All films were deposited using an electron cyclotron resonance (ECR) plasma source; that is, intrinsic mc-Si, n-type mc-Si, and dielectric silicon dioxide were grown with the ECR high density plasmas and the deposition rates for these films were in the range of 120 - 150 Å/min. The substrate temperatures during these depositions were maintained below 285 °C. When annealing was employed, it was done at 340 °C.

To fabricate the TFTs, we developed a repeatable and simple device fabrication flow; i.e., only two masks and one alignment step were employed for proximity-type lithography and no critical etching was involved during processing flow. Figure 1 shows the schematic of the device fabricated. The source/drain (S/D) contact metal (chromium) was deposited on top of n-type doped layer. The source and drain (S/D) regions were patterned by lithography and the patterns were defined by reactive ion etching. An 1800 Å intrinsic mc-Si and a 2000 Å silicon dioxide gate dielectric layers were subsequently deposited on top of the S/D contact using the ECR-PECVD without breaking vacuum. The film growth rates for mc-Si and oxide thin films were 120 Å/min and 150 Å/min, respectively. The intrinsic mc-Si layers were examined with XRD and Raman spectroscopy. During the HDP depositions, the substrate temperatures were maintained below 285 °C. The gate metal (aluminum) was evaporated on top of the gate dielectric. The gate region was defined using the lithography. The intrinsic mc-Si and the gate oxide were etched away from the top of the S/D contact region using the photoresist on the gate electrode as the mask. $CF_4/Ar/H_2$ and $CF_4/Ar/O_2$ gases were used to etch SiO_2 and mc-Si films, respectively. The etch end point was determined when the S/D contact metal became visible, and the electrical conductivity of this layer was measured as a verification for the etch end point.

Direct Deposition onto Plastic--Micro-crystalline Si TFTs: Results and Discussion

Figure 2 shows the transfer characteristics (V_g versus I_d) and transconductance (G_m) of an as-processed mc-Si TFT for V_d = 1V. All of thin films used for the TFT were deposited at temperatures lower than 285 °C and the deposition rates were ≥ 120 Å/min. It is noted that the although depositions are done at low temperatures, the film growth rates of intrinsic and n-type mc-Si layers are faster than the deposition rates of some other mc-Si films using RF driven hydrogen diluted plasmas. As seen in Figure 2 , the off-current is ~$3x10^{-13}$ A (~$2.5x10^{-14}$ A/μm) and the on/off current ratio is ≥ 10^6.]. The mc-Si TFT of Figure 2 performs with linear field effect mobility of 1.7 cm^2/V-s. The sub-threshold swing is ~0.2/decade and the threshold voltage is ~ 5V.

Figure 3 displays the transfer characteristics (V_g versus I_d) and transconductance (G_m) of the mc-Si TFT processed at < 285 °C and annealed 340 °C in forming gas when V_d is 1V. We note that the on-current is increased by an order of magnitude, and the transconductance is also increased correspondingly compared to the characteristics shown in Figure 2. The annealed TFT in Figure 3 shows linear field effect mobility of 12 cm^2/V-s, on/off current ratio of ~10^6, sub-threshold swing is ~0.3/decade, and threshold voltage of ~ 5V. After the annealing, the off-current minimum (~$4x10^{-13}$ A/μm) is increased by an order of magnitude and the off-current shows an electric field dependence.

Direct Deposition onto Plastic--Micro-crystalline Si TFTs: Conclusions and Recommendations

This work shows the promise of the HDP approach for directly depositing silicon onto plastics for all low-temperature processing silicon TFTs. Although the microcrystalline silicon thin film transistors we produced have been fabricated on glass substrates at low temperatures (<285 °C) using an ECR high-density plasma source, clearly the temperatures used are compatible with many plastics.. The deposition rates for n-type doped silicon, silicon dioxide, and intrinsic silicon layers were all in the range of 120 - 150 Å/min. This whole TFT fabrication procedure used only two masks and one alignment and no critical etch step was involved. When annealed at 340 °C mc-Si TFT has linear field effect mobility of 12 cm^2/V-s, on/off current ratio of ~10^6, off-current of ~ $4x10^{-13}$ A/μm, and threshold voltage of 5V.

Clearly this is a viable approach to Si TFT fabrication on plastic that can be fully developed. The steps we believe need further work principally involve stress control and plastic deformation problems impacting lithography. We believe the best approach to addressing these problems is to side-step them and move to a separation-based approach as discussed in the next section. This side-steps dimensional integrity issues on plastics and allows truly high performance silicon TFTs to be on plastic. This can be acheived since high processing temperatures can be used in the TFT fabrication before the TFTs are transferred to their flexible, plastic substrate.

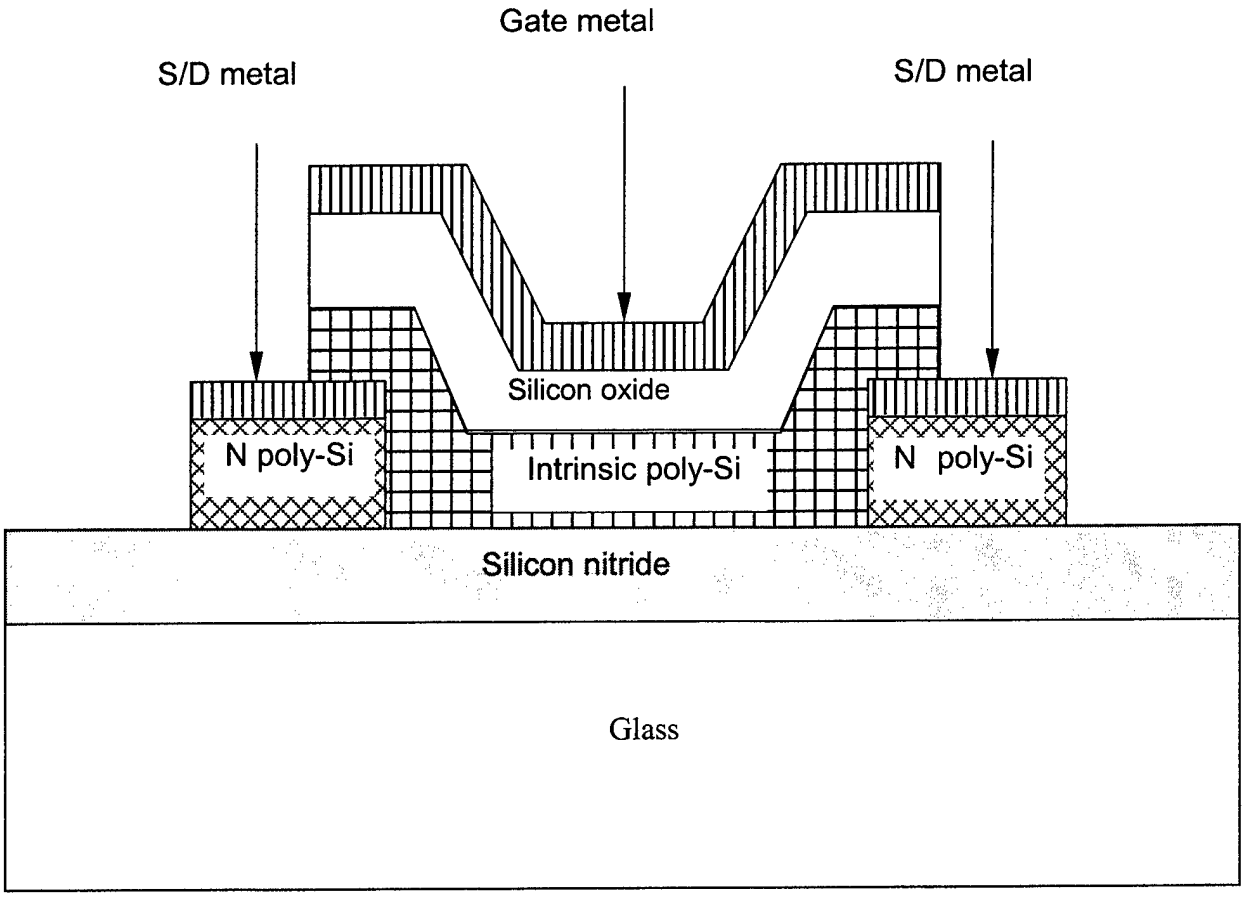


Figure 1. Schematic of mc-Si TFTs fabricated using the processing scheme described in the text.

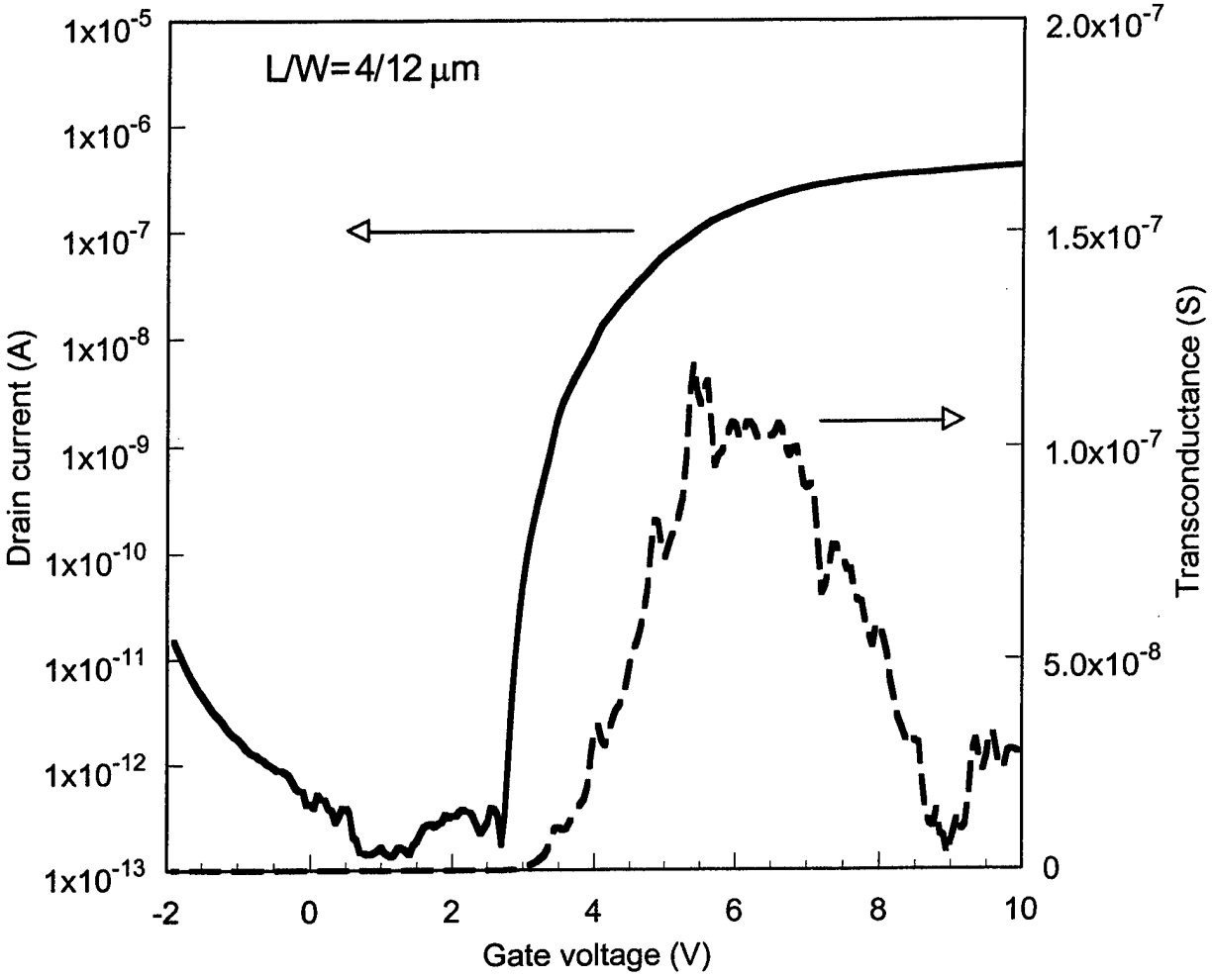


Figure 2. Transfer characteristics and transconductance of as-processed mc-Si TFTs when V_d = 1V. The substrate temperatures were maintained below 285 °C during the HDP depositions.

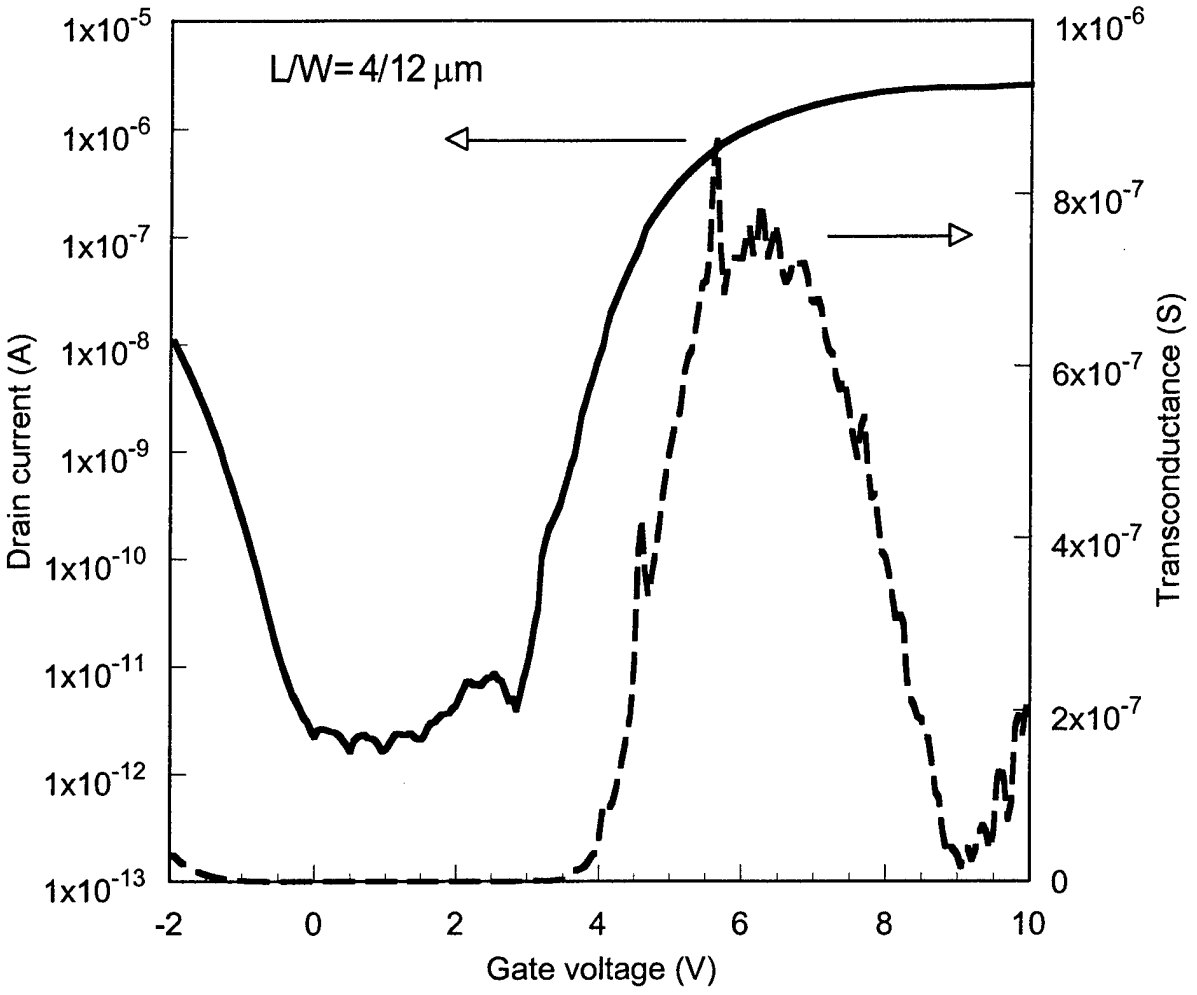


Figure 3. Transfer characteristics and transconductance of the mc-Si TFTs for V_d = 1V after a forming gas annealing at 340 °C for 1 hour.

3.1.1.2 High Performance Si TFTs on Plastic Using Separation Technologies: Introduction and Methodology

Poly-Si TFTs on flexible plastic substrates are of considerable interest due to their light-weight, flexibility, shock-resistance, and low cost for large area electronics, such as wearable/mobile information displays for civil and military applications. However, the fabrication of high performance transistors on plastics is extremely challenging for following reasons. First of all, the maximum process temperature must be lower than the plastic substrate's glass transition temperature (typically <300C), which is too low in comparison to silicon processing temperatures (>550 °C) generally regarded as being needed for high performance. This inherent temperature limitation leads to relatively poor field effect mobility and instabilities in such transistors. Second, due to a microscopically rough and uneven surface of most plastics, it is difficult to adopt conventional microelectronic processing techniques like lithography and surface planarization. Finally, device processing on flexible substrates can suffer from a lack of reproducibility and manufacturability due to their general mechanical and thermal instabilities during fabrication processing.

Given the fact that realization of any high performance TFT fabricated on plastic is limited by the plastic substrate itself, we are developing an entirely different approach, which decouples high temperature processes from the plastic materials involved. Our approach is based on a separation-process after the completion of device fabrication on some, large-area conventional substrate such as quartz or aluminosilicate glass. This separation process literally liberates the process and what it can attain from the inherent limitations of plastics. Figure 4 depicts the general process flow of our separation technology.

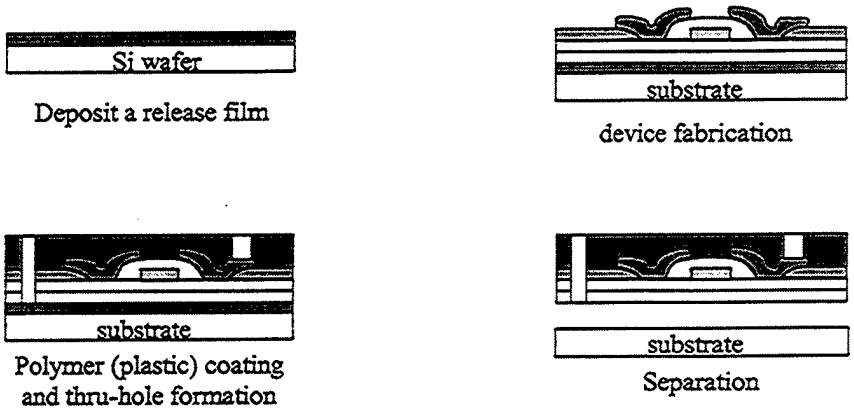


Figure 4. Schematic of our fabrication process flow for high performance poly-Si TFT on plastics.

High Performance Si TFTs on Plastic Using Separation Technologies: Results and Discussion

In implementations of this separation approach, as Figure 4 shows, we have been using silicon wafers as the "mother" substrate, from which separation occurs. In our most common approaches to date, prior to device fabrication, a release (sacrificial) layer is deposited on the oxidized silicon wafer "mother substrate". For this critical sacrificial layer, we have been exploring (1) an as-deposited high surface-to-volume ratio film (porous silicon), (2) a pre-made micro-channel structure, and (3) a self-assembled nano-silica beads release layer. After formation of the release layer on the mother substrate, the TFT device fabrication process flow takes place as follows. A 2000Å thick silicon oxide capping layer is deposited on top of the release structure using an ECR-PECVD system. A 1000Å thick a-Si precursor film is deposited in a low pressure chemical vapor deposition (LPCVD) system using SiH4 source gas at 300mT and 530°C with SiH4 source gas. Metal (nickel) seed patterns are formed on the precursor film and annealed at 570°C for metal induced crystallization (MILC). During the MILC process, polysilicon crystals grow laterally in the direction of carrier transport in the channel region, which results in polysilicon grain structure virtually free of large angle grain boundaries. The active region is isolated using optical lithography and reactive ion etching (RIE). A 1000Å thick gate oxide is grown on the active region using a diffusion furnace with dry oxygen gas and TCA at 1100°C. Then a 2700Å thick gate electrode silicon film is immediately deposited at 530°C with the same tool used for active film deposition. After patterning the gate electrode, the source and drain are doped with boron (33 KeV, 1E15cm-2) and phosphorous (80 KeV, 1E15cm-2) ion implantations for the p-channel and n-channel TFTs respectively. The dopants are activated by furnace annealing at 850°C for 30 minutes in a nitrogen ambient. The gate electrode is solid phase crystallized (SPC) at the same time as this activation annealing. Metal (aluminum) contacts for source, drain, and gate electrode are formed after opening the contact windows using lithography and oxide wet etching.

Figure 5(a) and 5(b) show transfer characteristics of a n- and p-channel TFT, respectively, fabricated using the fabrication process described above before separation. Table 1 is a summary of electrical performance of the transistors.

Once the TFT device is fabricated, Figure 4 shows that a polymer layer is then deposited on the surface, thru-holes are made, and the devices are separated. We have been developing several release layer/structures including as-deposited high surface-to-volume ratio (porous) films, micro-channel structures, and self-assembling bead release layers. Both a front- and back-side through hole method have been demonstrated to work for separation of a patterned active layer. Figure 6 shows top optical micrographs at various stages of separation processing using the micro-channel structure release approach. Figure 7(a) is a schematic view of the porous silicon sacrificial layer/front side through hole method. Figure 7 shows the separated plastic with an active pattern on it. Figure 8 is SEM micrograph showing self-assembled mono-layer of 210 nm silica beads on a chemically treated (functionalized) silicon wafer surface. This mono-layer of the beads is used for release layer exploiting its very high surface-to-volume ratio.

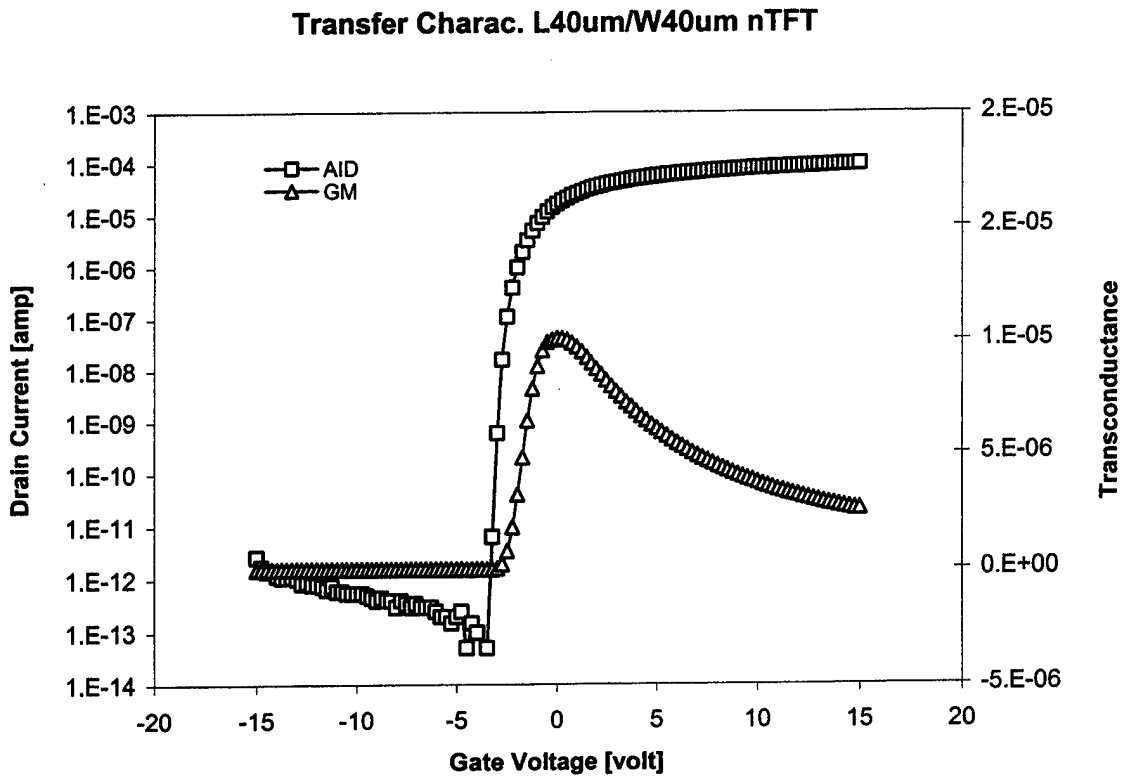


Figure 5(a). Transfer characteristics of a high temperature n-channel poly-Si TFT at Vds = 1 V.

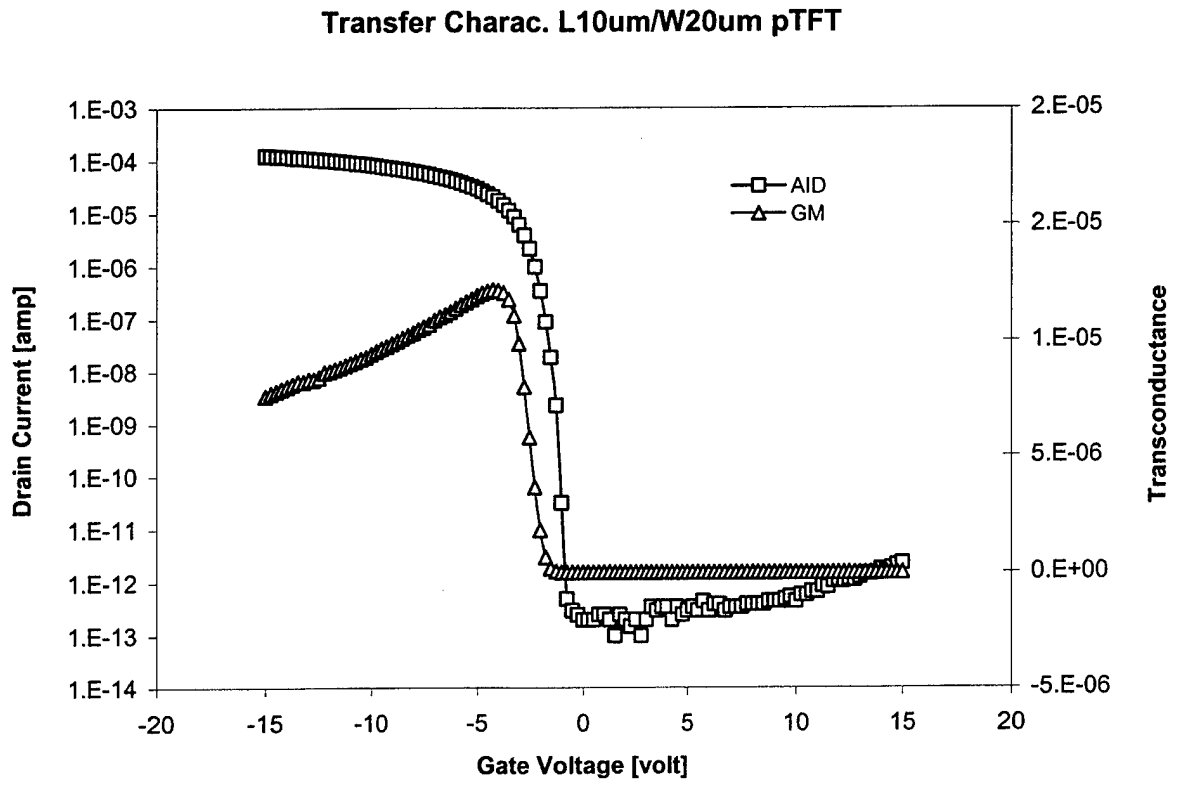


Figure 5(b). Transfer characteristics of a high temperature p-channel poly-Si TFT at Vds = 1 V.

Table 1. Summary of electrical performance of n- and p-channel transistors.

	Linear field effect mobility	on/off current ratio	sub-threshold swing	Vt by linear extrapolation
n-TFT	**293 cm2/V-sec**	**10^9**	**~180mV/dec**	**~ 0V**
p-TFT	**177 cm2/V-sec**	**10^9**	**~200mV/dec**	**~-3V**

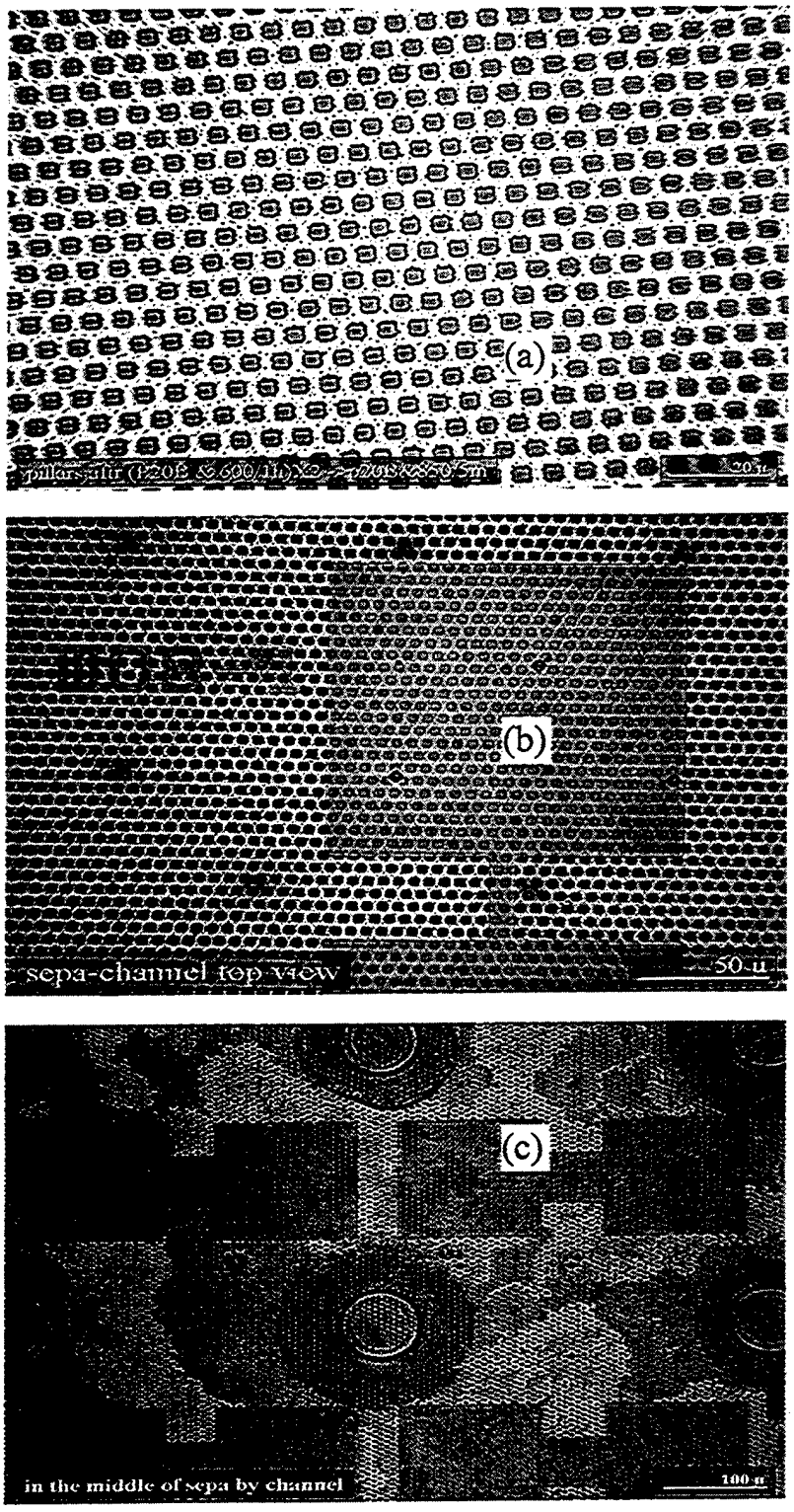


Figure 6. Top view of separation by micro-channel at various stages of processing; (a) micro-channel formation before device processing, (b) active pattern on the channel structure, (c) during separation after plastic coating.

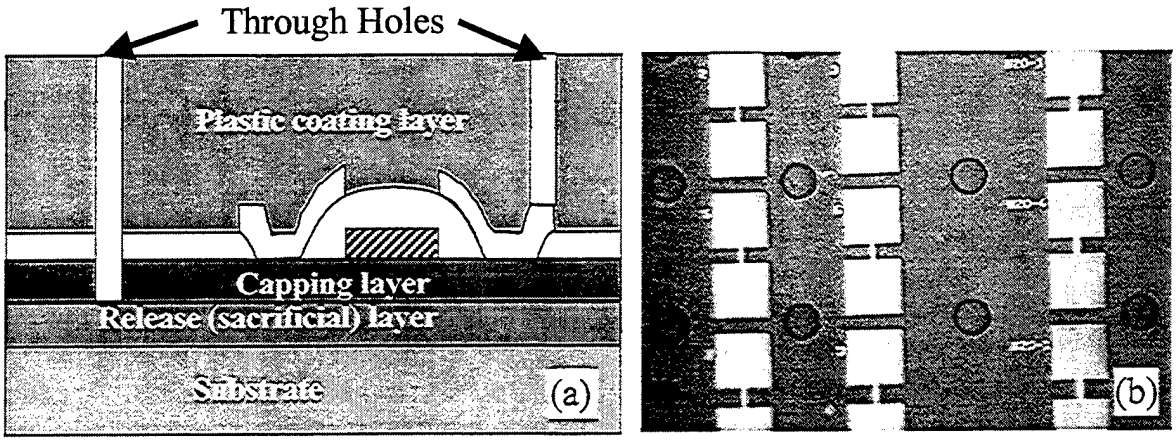


Figure 7. (a) schematic view of porous silicon sacrificial layer/front side through hole method; (b) resulting plastic layer with active pattern.

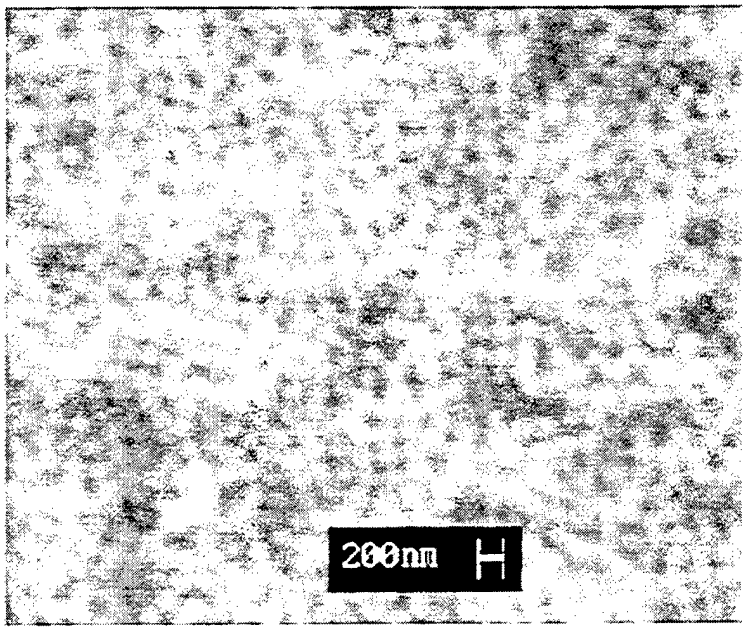


Figure 8. Scanning electron microscope (SEM) micrograph of a self-assembled silica bead (200 nm) monolayer assembled for device separation.

High Performance Si TFTs on Plastic Using Separation Technologies: Conclusions and recommendations

This approach of using a separation (release) layer allows the TFT processing to be divorced from the constraints of direct TFT circuit fabrication on plastics. It is the approach to take for truly high performance Si TFTs on plastics. Since our "mother" substrates are materials such as glass and quartz, large area devices can be fabricated without the need for tileing. Our approach is built on the concept that the "mother" substrates will be reused.

3.1.1.3 Low processing Temperature Dielectrics for Plastic Substrates (Gate, interlayer, and encapsulation layer uses) : Introduction and Methodology

Low processing-temperature dielectrics are critical for any circuit and display or detector/sensor array applications on plastic substrates since these materials are needed for gate, interlayer, planarization, and encapsulation layer uses To insure we have materials for these needs, we developed several paths to low temperature dielectrics. These paths are (1) low-processing temperature high density plasma (ECR) silicon oxide and nitride deposition based on silane as the precursor and (2)) low-processing temperature conventional RF plasma silicon oxide deposition based on trimethalsilane (TMS) as the precursor.

The efforts on developing low-processing temperature high density plasma (ECR) silicon oxide and nitride deposition based on silane as the precursor have been highly successful and are now well documented in the literature. Hence this work will not be discussed again.. We will report here on the TMS-based material which we have found has tunable conformality and stress properties.The low temperature silicon dioxide TMS-based thin films were prepared by plasma-enhanced chemical vapor deposition (PECVD). This TMS deposition was done at 100–200°C in the pressure range of 2–8 Torr.

Low processing Temperature Dielectrics for Plastic Substrates: Results and Discussion

The PECVD reactor as illustrated in Figure 9 was used for all the oxide preparation in this study. This reactor was equipped with the showerhead about 2 cm above the sample stage. Reactant gases, including ultra high purity (99.999%) oxygen and 99.9% TMS were mixed before being injected to the showerhead. In order for the film stress to be measurable and for better measurement accuracy, special p-type (100) Si wafers as thin as 37 μm were employed as the substrate in the stress testing. PECVD TMS oxide films with various thickness in the range of 1500-4500 Å were prepared to study the variation of stress with the film thickness and deposition conditions. For the evaluation of thin film conformality, PECVD TMS oxide films with a thickness of about 2000-3000 Å were deposited on the trenches precoated with 500 Å aluminum. The trench depth is approximately 0.4 μm and the trench width is about 0.8 μm. Deposition was performed in the substrate temperature range of 100–200°C, and the pressure range of 2–8 Torr. The TMS:O_2 flow rate ratio and RF power were chosen to be 1sccm:500sccm and 40 W, respectively. The deposition rate was about 2.3–5.7 Å/sec.

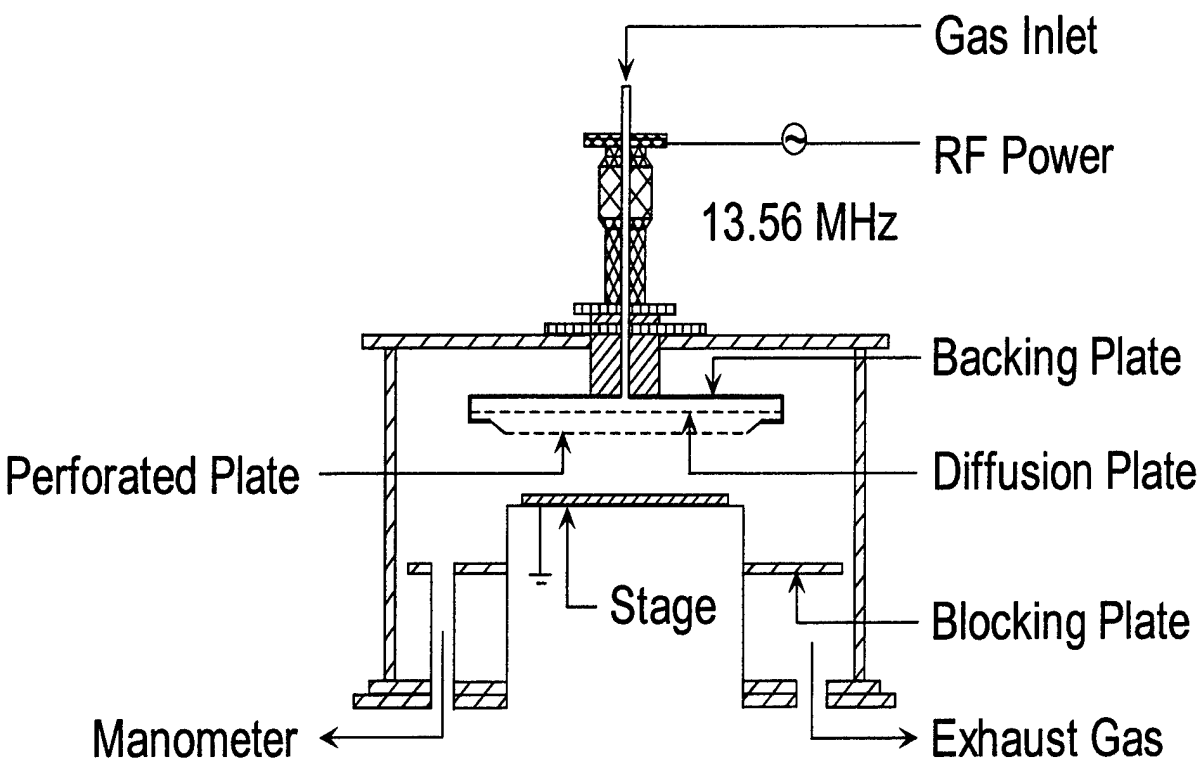


Figure 9. Schematic of the PECVD shower head configuration.

Stress Study

In this study, the measured stress σ_{tot} in the deposited film can be calculated by way of the Stoney formula

$$\sigma_{tot} = \frac{E_{sub}}{1-\nu_{sub}} \frac{t_{sub}^2}{6t_f}\left(\frac{1}{R_a} - \frac{1}{R_b}\right), \tag{1}$$

where the condition $t_f << t_{sub}$ and an isotropic distribution of the stress in the film cross-section have been utilized. In this equation, E_{sub}, ν_{sub}, and $E_{sub}/(1-\nu_{sub})$ are Young's modulus, Poisson's ratio, and biaxial Young's modulus of the substrate, respectively, t_{sub} and t_f are substrate and film thickness, respectively, R_a and R_b are the sample's radius of curvature after and before film deposition, respectively.

The film stress σ_{tot} consists of thermal stress σ_{th} and intrinsic stress σ_{ins}. The corresponding thermal stress can be expressed as a function of deposition temperature T_{dep}

$$\sigma_{th} = \left(\frac{E_f}{1-\nu_f}\right)(\alpha_f - \alpha_{sub})(T_{dep} - T_{mea}), \tag{2}$$

where E_f, ν_f and $E_f/(1-\nu_f)$ are Young's modulus, Poisson's ratio, biaxial Young's modulus of the film, respectively, α_f and α_{sub} are thermal expansion coefficients of the film and substrate, respectively, T_{mea} is the stress measurement temperature. In this study, E_f, ν_f were approximated to be 83 Gpa and 0.167 for all the PECVD TMS oxide films considered . The α_f and α_{sub} of this study were taken to be those of silicon dioxide and silicon. α_{Si} is reported to vary with temperature, and α_{SiO_2} is believed to be a function of temperature as well. However, given the low deposition temperatures and small temperature span employed in the experiment, $\alpha_{Si} = 2.49\times10^{-6}$/°C and $\alpha_{SiO_2} = 5\times10^{-7}$/°C at room temperature were adopted to simplify the calculation of Eq.(2). With knowledge of σ_{tot} and σ_{th}, the intrinsic stress σ_{ins} can be calculated following the expression

$$\sigma_{ins} = \sigma_{tot} - \sigma_{th} . \tag{3}$$

Ideally, film stress is independent of film thickness. However, thickness dependence of stress in PECVD TMS oxide films can be observed in Figure 10, where oxide films were deposited at 150°C and 3 Torr. As shown in Figure 10, stress in oxide films is insensitive to film thickness when the oxide film is thinner than 2500 Å. In contrast, when the film thickness is greater than 2500 Å, film stress linearly decreases with increasing oxide thickness. A similar thickness dependence of film stress was reported by others, and it was attributed to the surface reactivity of the deposited films. In light of the thickness dependence of film stress demonstrated above, stress measurement is usually performed with the same film thickness as that in real applications. Since PECVD TMS oxide is a promising candidate as a gate dielectric for flat panel displays , and 1500 Å is the typical thickness for such applications, our investigation of film stress with respect to deposition conditions was mainly performed with 1500 Å oxide films.

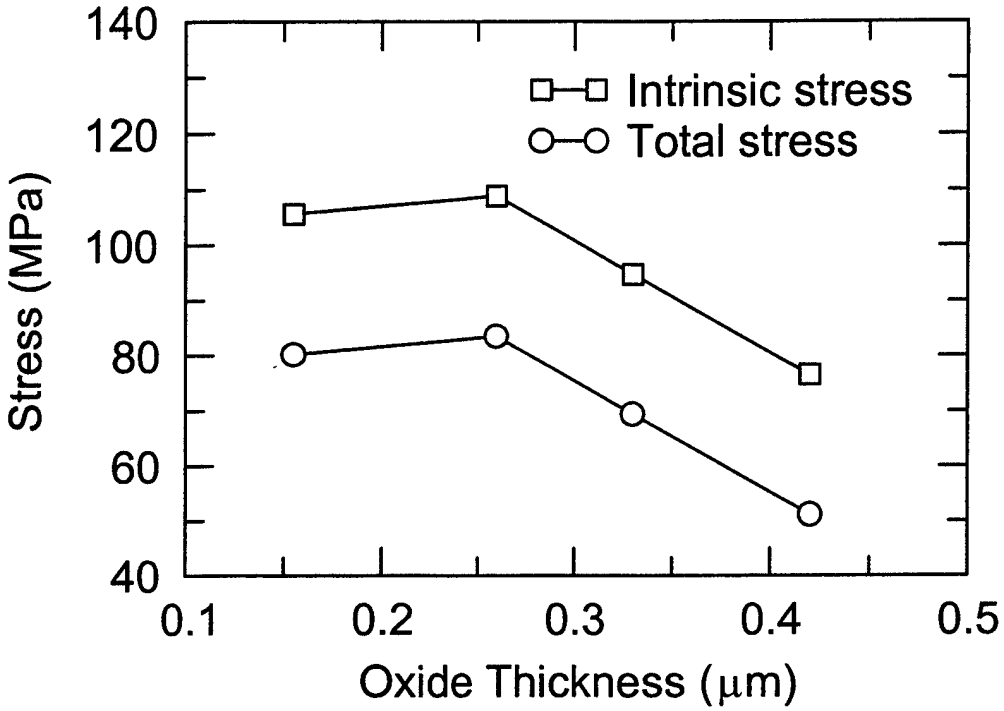


Figure 10. Total and intrinsic film stress as a function of film thickness. The PECVD TMS oxide films were deposited at 150°C and 3 Torr.

Figure 11 plots the total and intrinsic stress in the PECVD TMS oxide films as a function of deposition pressure. All the oxide films in this figure were deposited at 150°C. Tensile stress is observed in all the PECVD TMS oxide films. Both the total stress and intrinsic stress increase with deposition pressure. Due to the contribution of compressive thermal stress, the total stress exhibits a lower value of tensile stress than the intrinsic stress. Moreover, because all the samples in Figure 11 were prepared under the same substrate temperature, the contribution of compressive thermal stress is identical for all the samples; therefore, the intrinsic stress exactly follows the increasing trend of the total stress with deposition pressure.

The dependence of the total and intrinsic stress in PECVD TMS oxide films on the substrate temperature is shown in Figure 11, where all the oxide films were deposited at 2 Torr. It can be seen from the figure that both the total and intrinsic stress decrease with increasing substrate temperature. However, in contrast to Figure 11 where both the total stress and intrinsic stress exhibit exactly the same trend, the total stress in this case decreases somewhat faster than the intrinsic stress. As the substrate temperature increases, a larger differential temperature between deposition and measurement results in a more negative thermal stress, which accounts for the stronger temperature dependence of the total stress than the intrinsic stress. In addition, the total stress changes from tensile to compressive when the substrate temperature increases from 100°C to 200°C, and it approaches zero stress when the substrate temperature is about 190°C.

The trends observed in Figure 11 and Figure 12 can be understood in view of the film density and the incorporation of hydrogen into the oxide films in the form of Si-OH bond. FIIR spectra indicate that the Si-OH bond concentration in the oxide film increases with the deposition pressure, but decreases as the substrate temperature is raised. Consequently, the oxide film becomes less dense when deposited at a high deposition pressure or at a low substrate temperature which was verified by wet-etch rate and refractive index studies. From the deposition mechanism point of view, this is due to the relative contribution of ion-induced deposition which increases with the substrate temperature but decreases when the deposition pressure increases. The bombardment by energetic ion species aids in eliminating hydrogen from the growing film and improving the film density. This experiment demonstrated that, the type of stress and the stress level of PECVD TMS oxide films can be tailored as desired by changing the deposition conditions and film thickness. Moreover, the stress that exists in PECVD TMS oxide films is rather moderate. It should not raise any major functionality, manufacturability, and reliability concerns in most low temperature applications.

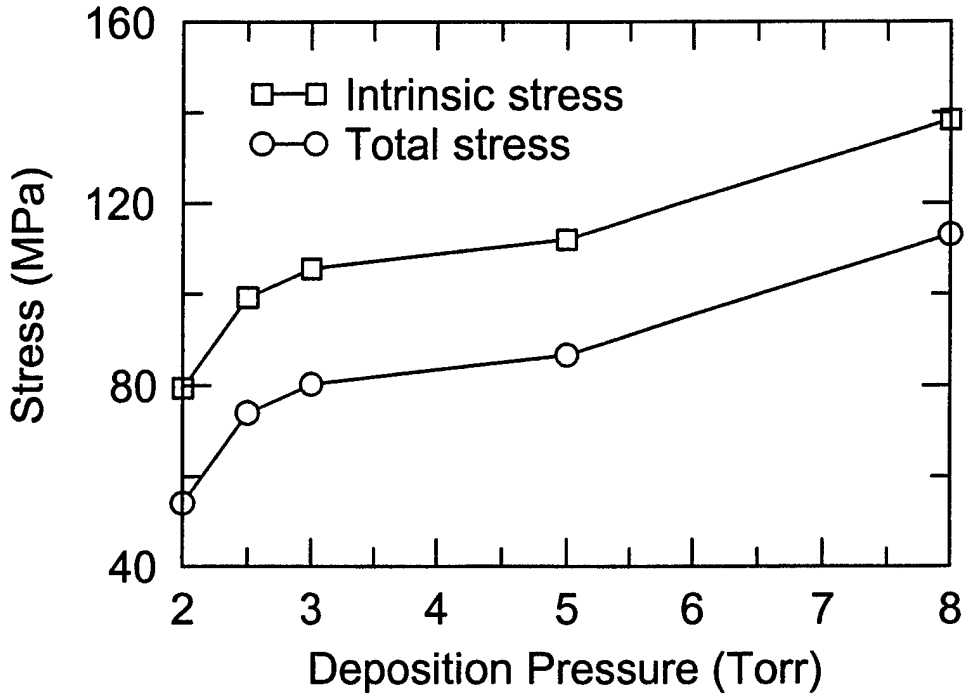


Figure 11. Total and intrinsic film stress as a function of deposition pressure. The PECVD TMS oxide films were deposited at 150°C.

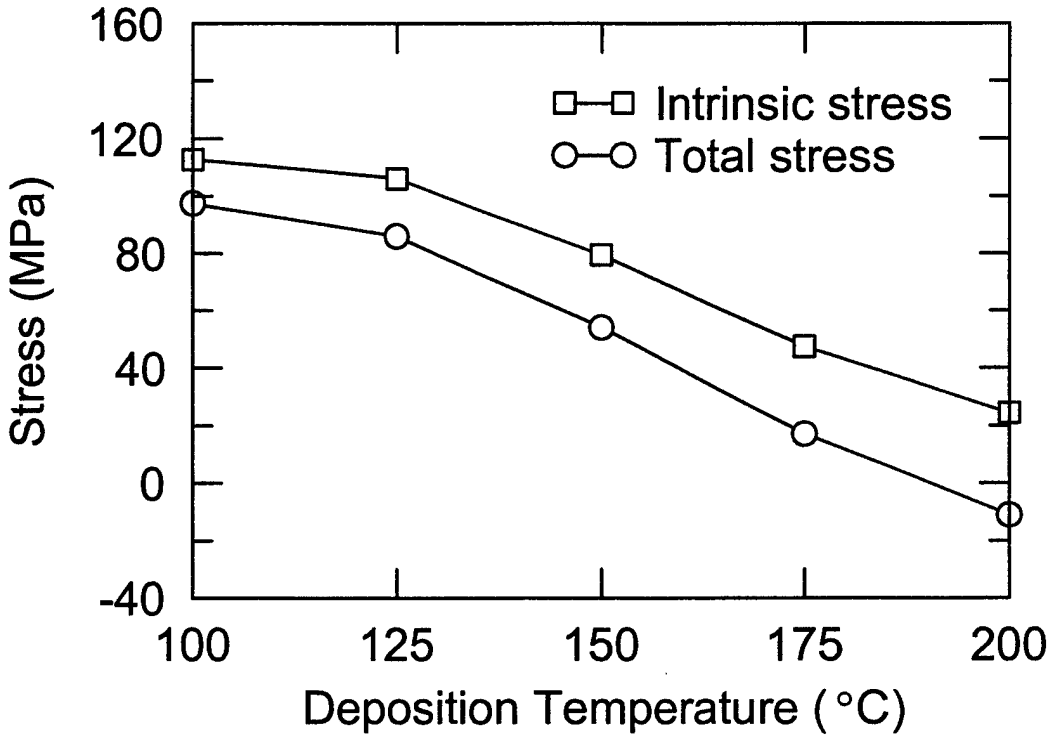


Figure 12. Total and intrinsic film stress as a function of substrate temperature. The PECVD TMS oxide films were deposited at 2 Torr.

Conformality

The conformality of PECVD TMS oxide films with various deposition conditions is shown in Figure 13. A representative XSEM micrograph of a trench filled with PECVD TMS oxide deposited at 200°C and 2 Torr is given in Figure 13(a). In this case, the oxide film on the external surface near the feature is thicker than those on the sidewalls and on the bottom of the trench. Meanwhile, film thickness on the trench sidewalls gradually decreases from the top to the bottom. In addition, thick cusps are present. The relatively poor conformality arises from an interplay of surface mobility and the significant role of ion-induced deposition at a high temperature and a low deposition pressure. The ionic species with a relatively high sticking coefficient are accelerated to the oxide surface by the sheath voltage; hence, their movement possesses directionality with a component perpendicular to the flat substrate surface. As a result of this directionality and the relatively high sticking coefficient of the ionic reactants, the ion-induced deposition tends to be non-conformal on topographical features such as in trenches. The thick cusps at the top corners indicate species surface movement from the top plane and trench sidewalls or that the deposition rate at the top corners is higher than that at the external surface of the trench or both. The enhanced deposition at the top corners could be due to re-emission of reactive ions from the sidewall near the trench top. When the substrate temperature decreases to 100°C, the following improvements are shown in Figure 13(b): (1) the oxide thickness difference between the external and internal surfaces of the trench becomes smaller; (2) the variation of oxide thickness along the trench sidewalls is not as significant as that shown in Figure 13(a) for the oxide deposited at the same deposition pressure but at a higher substrate temperature; (3) the cusps at the top corners of the trench become smaller. It is believed that a smaller relative contribution of the ion-induced deposition at a lower substrate temperature gives rise to the improvement in conformality. Besides the substrate temperature, the deposition pressure also influences the conformality via a shift in the deposition mechanisms. When the deposition pressure is raised from 2 Torr to 8 Torr, conformal oxide films can be attained, as shown in Figure 13(c). Figure 13 shows that the conformality of PECVD TMS oxide films varies dramatically with the deposition conditions. The good conformality of the oxide films demonstrated at 100°C and 8 Torr suggests that TMS is a promising candidate to replace TEOS as a Si precursor for low temperature inter-level dielectric deposition and for many other low temperature applications.

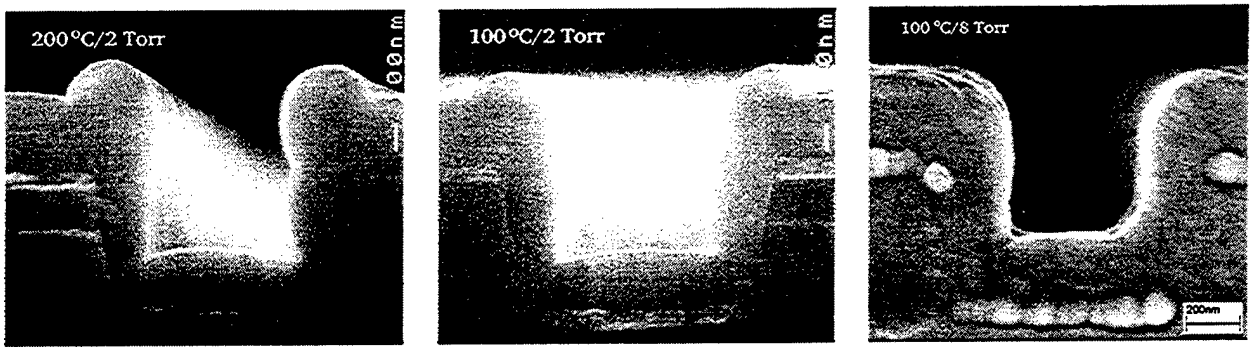


Figure 13. SEM of a trench filled with PECVD TMS oxide deposited at 200°C and 2 Torr (left), at 100°C and 2 Torr (center), and 100°C and 8 Torr (right).

Low processing Temperature Dielectrics for Plastic Substrates: Conclusions and recommendations

As noted, we found PECVD TMS oxide thin films deposited at these temperatures and pressures exhibit adjustable stress. The type of stress, including tensile stress, zero stress, and compressive stress, as well as the stress level can be tailored as desired by changing the deposition conditions and film thickness. In addition, the conformality of PECVD TMS oxide thin films was found to vary significantly with the deposition conditions. It improves when the deposition pressure is raised and the substrate temperature is reduced. The mechanisms for the variations of stress and conformality with respect to deposition conditions are discussed in this study. The adjustable stress and conformality of the PECVD TMS oxide make it a promising material for many low temperature applications such as inter-level dielectric, planarization, micro-electro-mechanical systems (MEMs) fabrication, and encapsulation.

3.1.1.4 Integrated Systems on Plastic: Introduction and Methodology

The specific goal we have had in Task 1 of this program is to bring all these enabling technologies together to create systems on flexible plastic substrates. Such systems may be detector arrays, molecular analysis arrays, such as that depicted in Figure 14, or simply displays. To make such systems a reality we have developed some unique materials that are fully compatible with use on plastics.

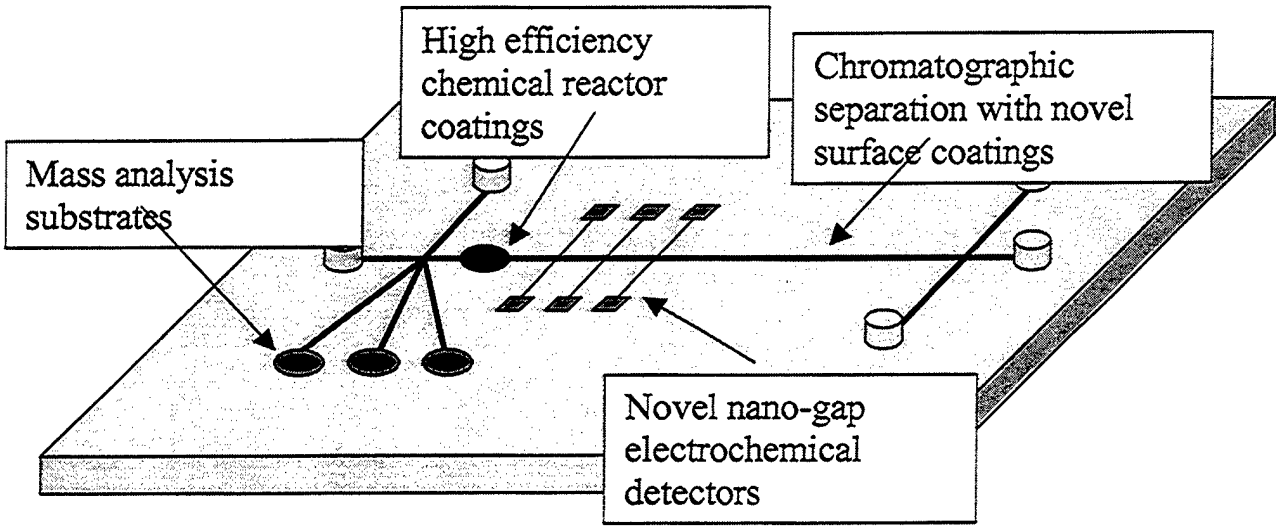
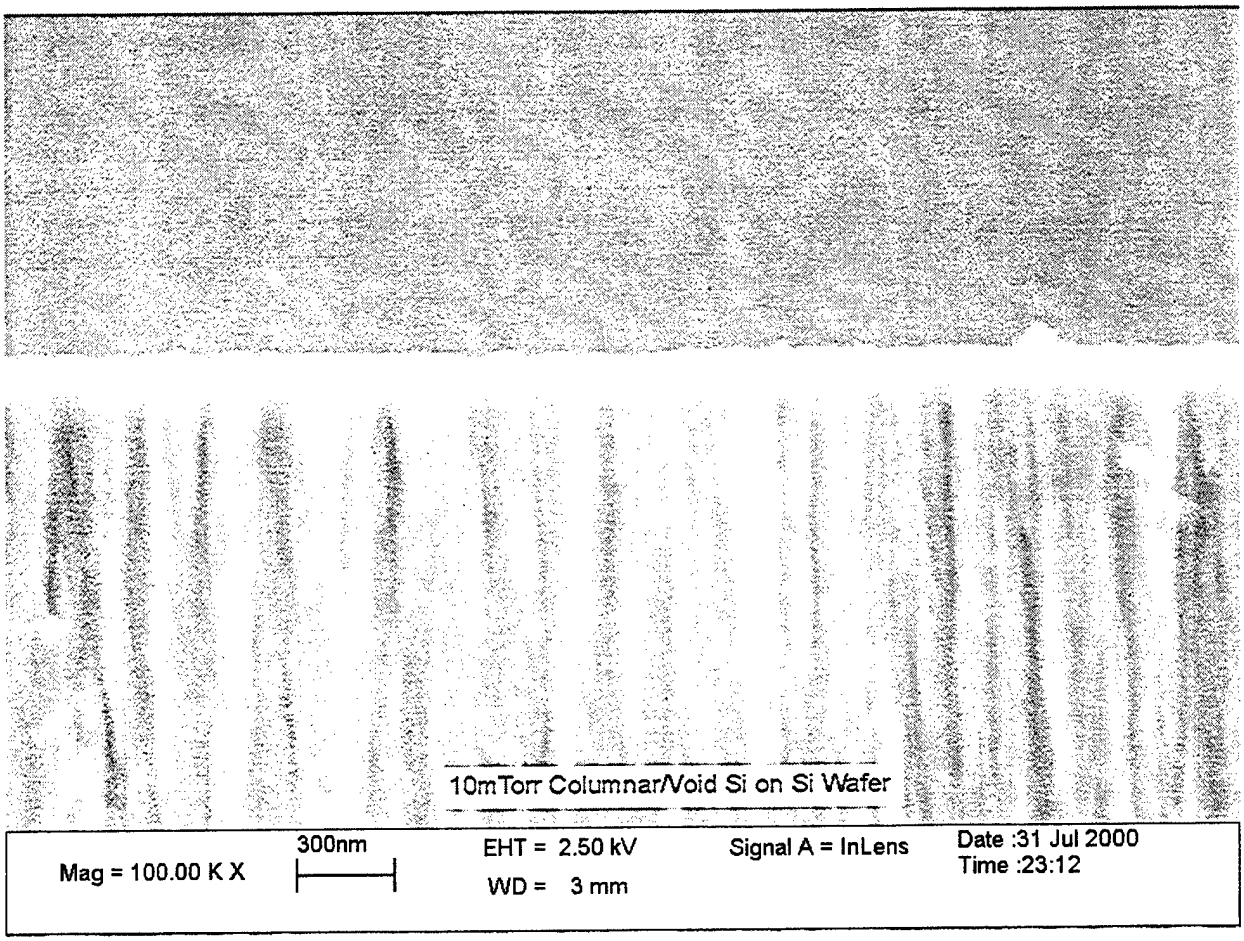


Figure 14. Analysis/detection array on a lightweight plastic substrate

Integrated Systems on Plastic: Results and Discussion

A material we have found to be fully compatible with deposition on plastics and to have a myriad of applications is our nano-structured column-void network deposited material seen in Figure 15. The nano-scale structure of this material enables its use in rapid molecular analysis (also seen in this figure) and this approach can then be integrated into the system depicted in Figure 14. Also we have already shown the material of Figure 15 has outstanding capabilities for gas detection uses as seen in the data of Figure 16. This demonstration is specifically of relative humidity detection and it points out how the systems of Figure 15, on lightweight plastics, could be an array of gas detectors. This detector structure of Figure 16 is the fastest, most sensitive relative humidity detector of any discussed in the open literature.



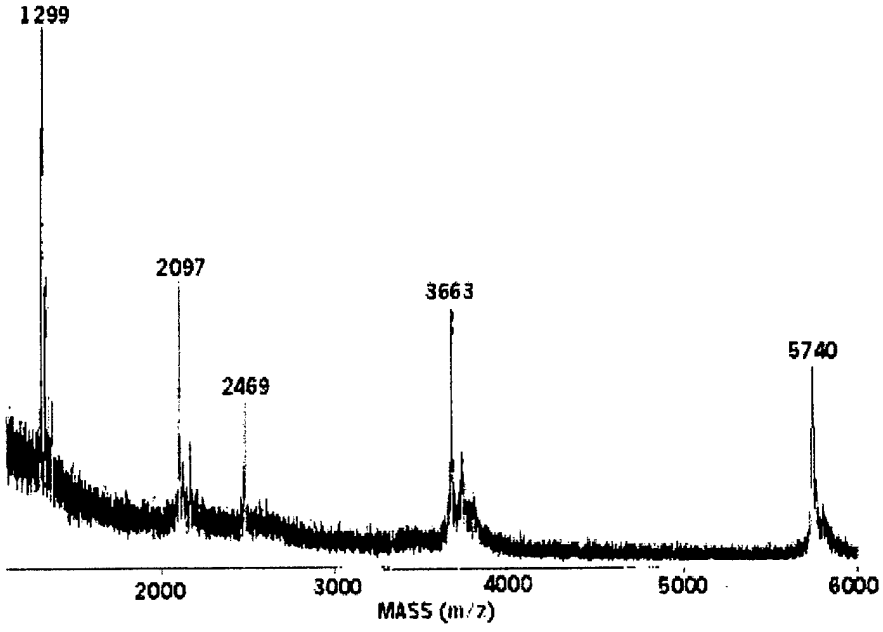


Figure 15. Molecular analysis (bottom) on a lightweight plastic substrate (top)

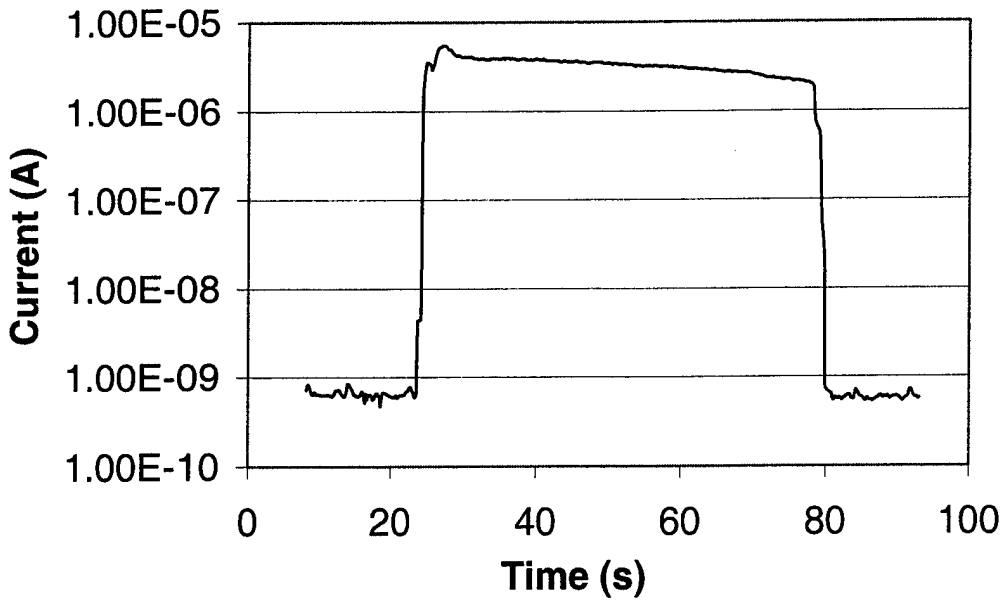


Figure 16. Gas detector (here water vapor) on a lightweight plastic substrate

To have systems such as those depicted in Figure 14 there must be an on-board power source. This too should be integrated into the system and it must be, therefore, a source that can be fabricated on or integrated into plastic laminates. We have fabricated two types of fuel cell structures to-date to provide this power. Type (1) and Type (2) are fabricated so that the starting material can be a deposited silicon film on plastic. All processing temperatures are compatible with that concept.

Type (1)

The first step in the fabrication flow(see Figure 17) for this approach is to deposit silicon nitride onto the Si which can be already established on a plastic substrate. The films are then patterned by photolithography and reactive ion etching. Then the exposed Si is etched by wet etching in chemicals, like KOH. As the result, a number of grooves can be made on Si. After this, a diffuser medium is bonded on the patterned Si wafer. We have used a ceramic with 200nm pores for the diffuser medium. We have used annealing to result in partial melting of a photoresist layer, which plays a role of glue between Si substrate and diffuser medium. Figure 18(a) shows the cross-sectional SEM photograph after bonding the diffuser medium on the groove-patterned Si wafer.

Membrane electrode assembly (MEA) is deposited on the diffuser medium. First, Pt thin film is deposited by e-beam evaporation, a physical vapor deposition method, on the diffuser medium. A thick electrolyte layer is deposited on the structure enough to form a continuous film on the porous diffuser medium. The ECR-PECVD method is used to deposit silicon dioxide film to form an electrolyte layer. Figure 18(b) is the bird's-eye view SEM picture of a fuel cell after electrolyte deposition. Again, the other electrode is deposited by evaporation followed by lift-off

procedure on the top of the electrolyte. Part of electrolyte is etched away allowing Pt exposed to the surface to become a terminal for signal readout.

To test this type (1) structure, a mixture of methanol and water is used. The fuel solution is supplied through the grooves in Si surface and the diffuser medium. The fuel meets the bottom electrode on the top of the diffuser medium and the reaction is carried out. Then, the bottom electrode is anode in this case and the top electrode will act as a cathode. In this configuration a value of 0.324V is observed from the fuel cell for the open-circuit voltage. A value of 0.867μA was measured as the short-circuit current. The I-V characteristic is measured by sweeping voltage. Figure 18 shows the I-V characteristic from a fuel cell of 20μm width and 2mm length channels. Maximum power is 113 nW/cm2 at 0.21 V.

Type (2)

In the Type (2) approach, the fuel cell is fabricated on the Si without the use of a diffuser medium and by utilizing micro-and nano-channels as the direct fuel supply means. The diffuser medium is eliminated in approach 2 and the fuel is supplied directly to the micro- and nano-channels. Figure 20 shows the schematic of the approach 2 micro-fuel cell. A thicker electrolyte layer was integrated for the fuel cell to provide the proton conducting medium, as well as mechanical support for the cathode and electrolyte itself over the micro- and nano-channels. After fabrication, the same measurement is carried out for the fuel cell. Approach 2 gave 0.4 V of open-circuit voltage and 0.4μA of short-circuit current. The maximum power is 25nW at 0.144 V. Figure 21 shows the I-V characteristic of the fuel cell fabricated by approach 2.

In approach 2, a thicker electrolyte layer has been used to-date but the electrode of approach 1 is still employed. In approach 1, the electrolyte thickness is 5000 Å compared to 3um in approach 2. The electrolyte is a proton conducting medium and its proton conductivity determines the number of protons passing through the electrolyte, hence the current flow through the electrolyte. Since both approaches have the same material for the electrolyte, approach 2 results in lower proton conductance and lower current output due to the thicker electrolyte.

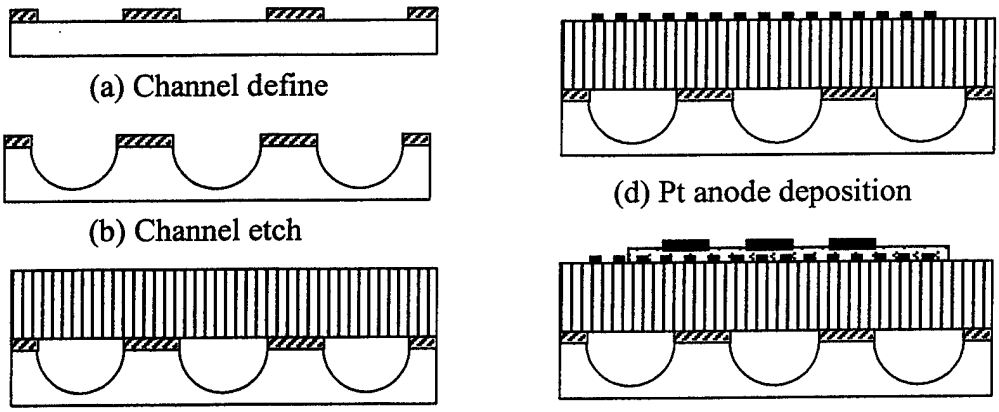


Figure 17. Process Sequence for Micro-fuel cell – Approach 1.

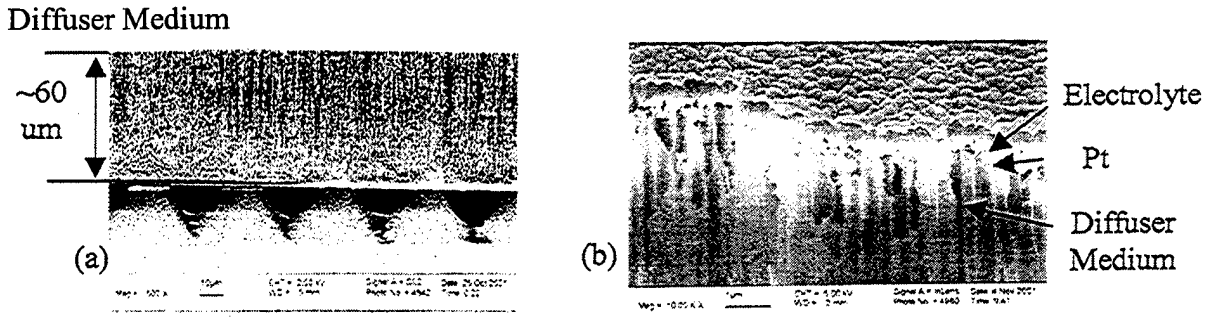


Figure 18. Integration of Porous Diffuser Medium.

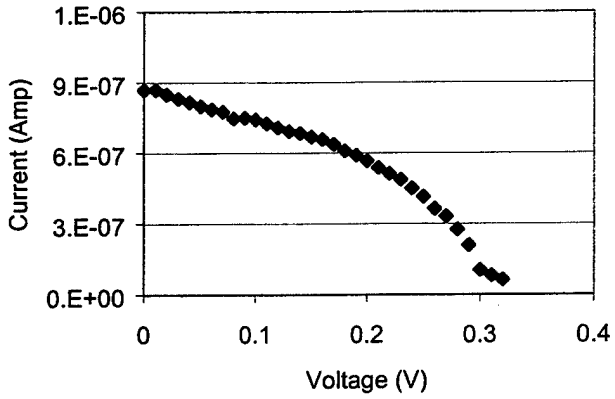


Figure 19. I-V Characteristics of Micro-fuel cell – Approach 1.

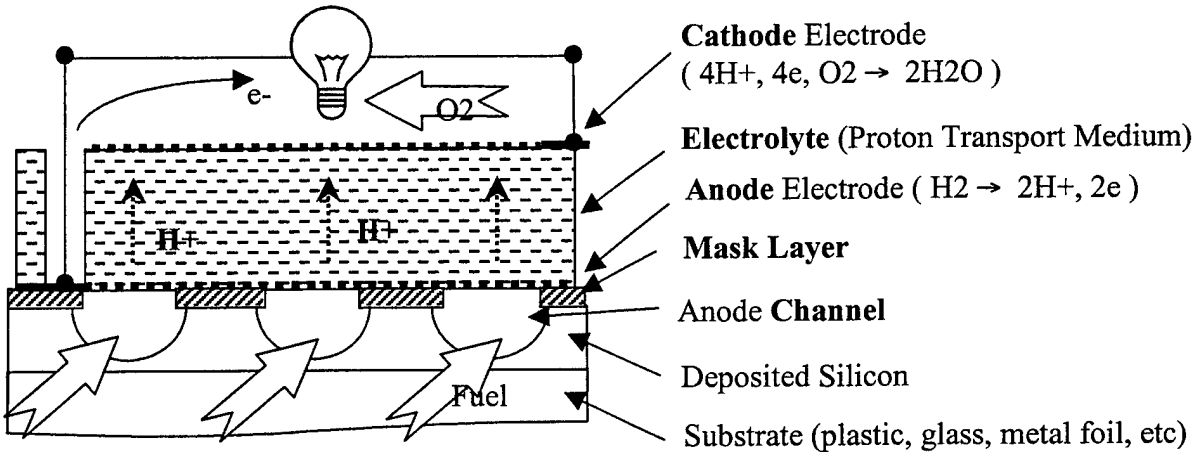


Figure 20. Schematic of Micro-fuel cell – Approach 2.

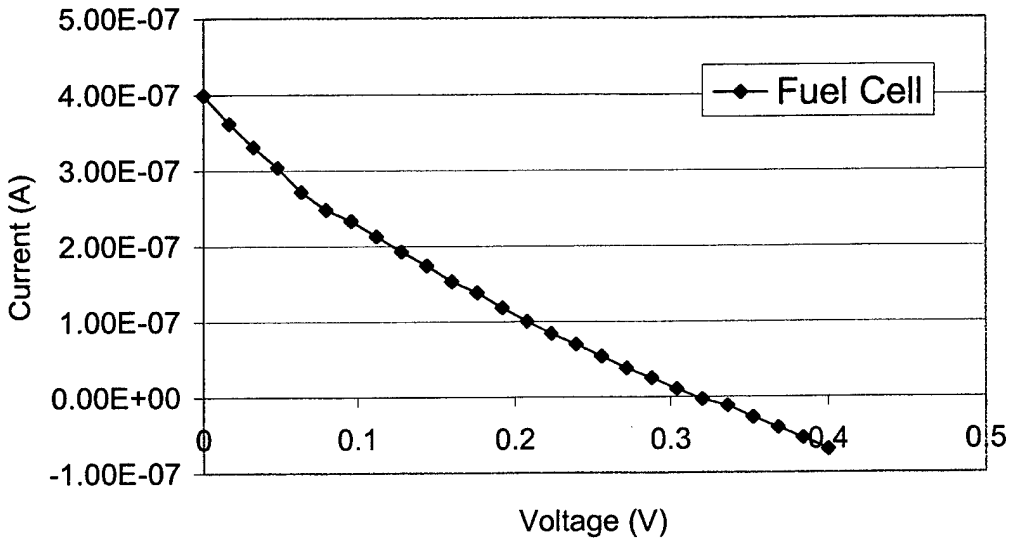


Figure 21. I-V Characteristic of Micro-fuel cell – Approach 2.

3.1.2 NOVEL SUBSTRATES AND ENCAPSULATION (Wagner – Princeton)

The ideal flexible active matrix backplane is rugged, rollable and bendable, capable of CMOS operation, and lends itself to low cost manufacture. TFT backplane technologies are categorized by their active semiconductor. To the expert this description serves as a summary of the entire backplane technology. Active semiconductors for TFT backplanes, rigid or flexible, include amorphous silicon and polycrystalline silicon thin films, silicon microblocks, II-VI compound semiconductors, and organic semiconductors in polymer and molecular form. As these technologies develop away from glass substrates toward deployment on flexible substrates, their description according to semiconductor is augmented by the specification of the substrate, the present task being no exception. In the silicon semiconductor / substrate matrix shown below as Table 2 the task occupies four fields.

Table 2. Compatibility of deposited thin film silicon TFT channel materials with substrate materials. The entries shown in bold were subjects of this task.

Substrate material⇒ ⇓ TFT application	Plastic ≤ 150°C	Glass ≤ 600°C	Steel ≤ 1000°C
Matrix switch (only *n* channel)	**a-Si**	a-Si	**a-Si**
Matrix switch and peripheral circuits (*n* and *p* channel)	**nc-Si**	poly-Si nc-Si	**poly-Si** nc-Si

We entered the current grant period with work in progress on amorphous silicon TFTs on plastic foil and on stainless steel foil. These are n channel devices that provide switches and other on-pixel functions. They are sufficiently well characterized to serve as the vehicles for evaluating the effect of mechanical deformation on the electrical performance of TFTs. However, on account of their inadequate hole field effect mobility a-Si TFTs cannot sustain p channel operation. Yet a fully integrated and therefore broadly applicable backplane needs a CMOS capable semiconductor. This was the main motive for pursuing the fabrication of polycrystalline Si on steel foils, and of nanocrystalline silicon TFTs at 150°C, which were grown into full research projects.

While the mechanical properties of thin films in wafer based silicon integrated circuits had attracted considerable attention, essentially no quantitative information existed on the interaction between mechanical deformation and electrical characteristics of TFTs on foil substrates. With interest in flexible displays on the rise, a predictive understanding of their electro-mechanical properties is becoming important. The goal of our work was to provide this information through experimental and theoretical studies.

A key to the successful completion of this task was the ability to deposit thin films of silicon, doped silicon, silicon nitride and silicon oxide at low substrate temperatures, and to process the materials to devices in a semiconductor fabrication facility. [1] In the following the state-of-the-art processes used for fabricating TFTs are described in detail.

3.1.2.1 Amorphous silicon TFTs on Kapton foil

Substrate selection

Using organic polymers as substrates for TFT electronics requires initial surface passivation. The passivation layer seals the polymer foil and converts the chemistry of the polymer to the chemistry of the passivating material. The passivation layer substantially reduces the possibility of the contamination of the TFT layers during their growth caused by outgassing, and oxygen and water release from the polymer foil. Importantly, the passivation layer also serves as the mechanical bond between the TFT layers and the substrate. [2]

During the TFT fabrication the polymer foil may be temporarily bonded to a rigid substrate, such as silicon wafer or glass, or processed as a free standing substrate. If it is bonded, the thermal expansion of the substrate during thermal cycling will be dominated by the coefficient of thermal expansion of glass/Si wafer, which is much lower than that of the polymer substrate and therefore is more suitable for TFT fabrication. This procedure still relies on a semi-permanent bonding agent during the TFT fabrication. After fabrication the polymer foil with the TFTs is detached from the rigid substrate. If a free standing polymer foil is used, its coefficient of thermal expansion becomes extremely important. In addition, the built-in stress in all TFT layers must be very well controlled. Excessive built-in stress or any mismatch in the coefficient of thermal expansion between any TFT layer and the polymer substrate may result in severe substrate curving. The free-standing foil approach is more suitable to future roll-to-roll manufacturing.

Following the above arguments, we selected polyimide Kapton®E as the substrate for a-Si:H TFT fabrication. Kapton has good chemical stability, shrinks by only ~ 0.03% when held at 200°C, has a relative humidity (RH) expansion coefficient of $9x10^{-6}$ per percent of RH, a water permeability of 4 $g/m^2/day$, an oxygen permeability of 4 $cm^3/m^2/day$, a coefficient of thermal expansion of $12x10^{-6}/°C$, a glass transition temperature ~ 350°C, and an RMS surface roughness of ~ 30 nm.

TFT fabrication

Our 150°C fabrication process of amorphous silicon (a-Si:H) thin-film transistors (TFTs) on Kapton E is performed on a free standing substrate passivated on both sides with SiN_x deposited by plasma enhanced chemical vapor deposition (PECVD). [3] We selected this temperature for two reasons: (i) several types of organic polymers can withstand the temperature of 150°C and therefore this technology can potentially be used on other substrates, and (ii) we show that the quality of the a-Si:H and SiN_x layers grown by PECVD at 150°C can be made comparable to that of the materials grown at higher temperature.

Standard a-Si:H TFT fabrication by PECVD requires deposition temperatures from 250 to 350°C. We have developed a technology where all TFT layers are deposited at ≤ 150°C. It is known that the quality of the amorphous silicon (a-Si:H) and silicon nitride (SiN_x) deposited by PECVD deteriorates with the decreasing deposition temperature. During growth at 150°C, the usual source gases are diluted with hydrogen to ensure that the electronic properties of a-Si:H and SiN_x layers are comparable to those of a-Si:H / SiN_x grown at the optimum temperature of 250-350°C [4,5].

We fabricated arrays of a-Si:H TFTs on 51 μm thick Kapton E at the maximum process temperature of 150°C. First, the polyimide substrate was coated on both sides with a 0.5 μm thick layer of SiN_x. The TFTs had a staggered bottom gate geometry with the channel pasivated by SiN_x. All TFTs had the following structure: ~ 100 nm thick Ti/Cr layer as gate electrode, ~ 360 nm of gate SiN_x as gate dielectric, ~ 100 nm of undoped a-Si:H as channel material, 180 nm of passivating SiN_x, and ~ 50 nm of (n^+) a-Si:H and ~ 100 nm thick Al for the source-drain contacts. The stress was optimized in all TFT layers to make the substrate come out flat after fabrication. The cross-sectional view of a-Si:H TFTs is shown in Figure 22. The transistors were annealed after the fabrication.

The fabrication and properties of the TFTs' component layers are described in detail below.

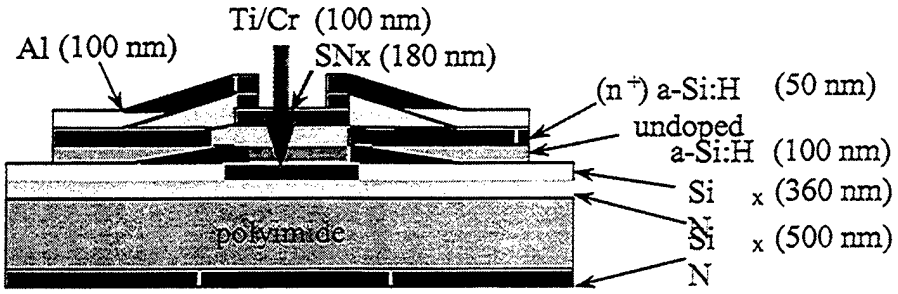


Figure 22. Schematic cross section of a back channel passivated a-Si TFT on a passivated polyimide foil substrate.

Silicon nitride deposition and properties

The SiN_x films were deposited from mixtures of SiH_4, NH_3 and H_2 using 13.56 MHz PECVD at a pressure of 500 mtorr (~ 67 Pa). All layers were deposited at 150°C and the silane and ammonia flows were kept constant at 5 sccm and 50 sccm, respectively. We varied the H_2 flow rate from 55 to 220 sccm and the plasma power from 5 to 50 W. The electrode area was ~ 250 cm^2. Each layer was simultaneously deposited on a clean Corning 7059 substrate (for optical measurements), on Corning 7059 coated with Cr (for electrical measurements,) and on a p-type Si wafer of [111] orientation (for infrared measurements). Most of the films were around 0.5 μm thick. We measured the growth rate, the index of refraction n (from optical transmission measurements using the Swanepoel method), the leakage current through the nitride (from I-V curves taken from –100V to +100V), the dielectric breakdown field, the dielectric constant ε at 1 MHz, the etch rate in 10:1 buffered oxide etch, the Fourier-transform infrared absorption (FT-IR) spectrum, the Rutherford back-scattering (RBS) spectrum, and the secondary ion mass spectrum (SIMS). Selected SiN_x recipes were then tested by fabricating inverted staggered a-Si:H TFTs with either the back-channel etch or the SiN_x channel-passivated structure.

Raising the hydrogen flow from 55 to 220 sccm, at a radiofrequency (RF) power of 5 W reduces the growth rate from ~ 1.6 to ~ 1.1 Å/s and increases the index of refraction from 1.75 to 1.79. At the hydrogen flow rate of 165 sccm, an increase in the RF power from 5 to 20 W causes an increase in the growth rate from 1.2 to 2.1 Å/s and a slight increase in the index of refraction from 1.79 to 1.80. At the highest hydrogen flow of 220 sccm, increasing the RF power from 5 to 50 W raises the deposition rate from 1.1 to 2.9 Å/s, and the index of refraction increases from 1.79 to 1.81.

As the hydrogen flow increases, the etch rate in 10:1 buffered oxide etch drops dramatically from 412 to 96 Å/s, indicating that the most dense films are deposited with the highest hydrogen flow. The dielectric constant of ~ 6.85 does not change much with hydrogen flow rates between 55 and 110 sccm, but for larger hydrogen flows it increases to a value of 7.38. With an increase in the RF power from 5 to 20 W, there is a large increase in ε from 7.14 to 8.49 and a decrease in the etch rate from 172 to 73 Å/s, again indicating that denser films are deposited at higher power. For the highest hydrogen flow, the etch rate and the dielectric constant do not vary much in the RF power range from 5 to 50 W. Up to 40 W the dielectric constant varies between 7.29 and 7.44 and reaches a value of 8.18 for the power of 50 W. The etch rate drops slightly between 5 and 20 W and above that it remains constant at a value of about 65 Å/s.

All films were tested in a sandwich configuration for leakage current and the dielectric breakdown field. The maximum voltage applied to the samples was 100 V. In the leakage current, no major differences were observed. All films easily withstand the applied electric field and in all cases the breakdown field is larger than 2 MV/cm.

FT-IR absorption spectra show the following main vibrational bands: N-H stretching band around 3340 cm^{-1}, Si-H stretching band around 2170 cm^{-1}, N-H_2 scissors around 1550 cm^{-1}, a band around 1190 cm^{-1}, and the Si-N stretching band around 890 cm^{-1}. While the size of most

IR bands does not vary much with changing hydrogen flow or RF power, the Si-H stretching band at 2170 cm^{-1} decreases with both increasing hydrogen flow and increasing RF power.

The Si/N ratio was measured by Rutherford backscattering (RBS), and the hydrogen concentration by secondary ion mass spectrometry (SIMS). The value of Si/N for a stoichiometric film is 0.75. All measured films are nitrogen rich and the Si/N ratio varies between 0.56 and 0.67. As the hydrogen flow increases, the films become more 'silicon rich' with higher values of Si/N. The dependence of the Si/N ratio on power is more complicated and appears to reach maximum of 0.67 at the RF power of about 20 W. The SIMS measurements reveal that the hydrogen content remains nearly constant at a value of $2x10^{22}$ cm^{-3} in the tested interval of hydrogen flow and RF power.

Optimized low temperature silicon nitride

Device quality SiN_x gate dielectric deposited at the standard temperatures of 300-350°C usually is slightly nitrogen rich. Nitrogen rich SiN_x results in better TFT characteristics and is more stable than silicon-rich SiN_x. Nitrogen rich SiN_x contains a large amount of hydrogen, 20-35 atomic %, with the larger fraction bound in N-H groups. The threshold voltage of the TFTs is lowest when the refractive index of the SiN_x layer lies in the range of 1.85 to 1.90. The index of refraction is related to the stoichiometry of the film, being larger for silicon-rich films. The etch rate in 10:1 buffered HF usually has a value of 20 Å/s. It decreases rapidly with increasing index of refraction n up to the value of about 1.83 and remains constant for higher values of n. The etch rate has been reported to rise with increasing concentration of bonded hydrogen in the film.

Based on the knowledge collected from the SiN_x films deposited at 300-350°C, the optimized low-temperature film should be slightly nitrogen-rich with low hydrogen content, low etch rate, high dielectric breakdown field, index of refraction of about 1.85, and preferably high growth rate. Following upon the above mentioned requirements, the SiN_x layer deposited from the gas mixture of 5 sccm of SiH_4, 50 sccm of NH_3 and 220 sccm of H_2, at the power of 20 W fulfills these requirements best. This film has a growth rate of 1.5 Å/s, etch rate of 61 Å/s, index of refraction n = 1.80, dielectric constant ε = 7.46, dielectric breakdown field > 3.4 MV/cm, Si/N ratio of 0.67, and H content of ~ $2x10^{22}$ cm^{-3}.

Optimization of back-channel etch a-Si:H TFTs

We fabricated a series of back-channel etch a-Si:H TFTs by depositing at 150°C on Corning 7059 glass or 51 μm thick Kapton E substrate, in the geometry shown in Figure 23. First, the polyimide substrate was coated on both sides with a 0.5 μm thick layer of SiN_x that serves as a diffusion barrier. All TFTs had the following structure: ~ 100 nm thick Cr layer as gate electrode, ~ 400 nm of gate SiN_x, ~ 200 nm of undoped a-Si:H, ~ 50 nm of (n^+) a-Si:H, and ~ 100 nm thick Cr layer for the source-drain. Using an identical recipe for all transistors, the undoped a-Si:H was deposited from a mixture of SiH_4 and H_2, and the (n^+) a-Si:H from a mixture of SiH_4, PH_3 and H_2. The optimized 150°C SiN_x recipe was used for TFTs deposited on both polyimide and glass, for comparison. Two other sets of TFTs with different SiN_x layers were

deposited on glass. For both sets, the gas flow rates during the SiN_x deposition were identical to the optimized recipe, but the RF power was reduced to 15 or 10 W.

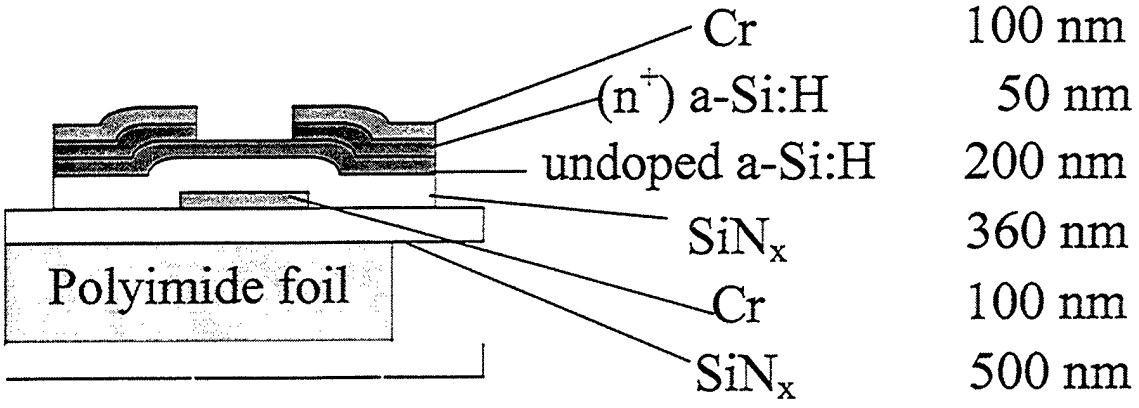


Figure 23. Schematic cross section of a back channel etched a-Si TFT on a passivated polyimide foil substrate. The bottom passivation is shown as an optional layer, in a configuration prepared for bending experiments.

Optimization of a-Si:H TFTs with channel passivation

Next, we chose the structure for the a-Si:H TFTs where the back side of the channel area is passivated with a SiN_x layer. The cross-sectional view of this structure is shown in Figure 22. This structure allows us to reduce the thickness of the a-Si:H channel layer while protecting the channel from the environment. All TFTs were deposited on Corning 7059 glass at 150°C using the same recipes as before. The SiN_x layer was deposited using the optimized recipe. In some TFTs we varied the amount of the hydrogen flow for either the SiN_x or the a-Si:H layer next to the SiN_x/a-Si:H interface, thus modifying the interface layer to a depth of about 20 nm. The TFT channel length was 40 μm and channel width was 400 μm. The gate dielectric was ~ 360 nm thick and the channel layer was either 100 or 200 nm thick. The transistors were annealed after fabrication.

As expected, the off-current is reduced by a factor of two when the channel layer thickness is reduced to one-half. The calculated linear mobilities reveal that the thickness reduction in the a-Si:H channel layer from 200 to 100 nm had the most pronounced effect on the mobility. A further slight improvement was achieved by raising the hydrogen flow during the growth of the a-Si:H layer, while a deterioration occurred when the hydrogen flow was raised to 330 sccm during the growth of the SiN_x gate dielectric layer. The threshold voltages are low and vary between 1.4 and 1.9 V. The values for the linear mobility and the threshold voltage are averaged over several devices.

In the last step we fabricated TFTs on 51 μm thick polyimide foil with procedures very similar to those for TFTs on glass. But before the TFT growth the polyimide was coated on both

sides with a 0.5 μm thick layer of SiN_x. The Cr layers, used previously for metallization, were replaced with more ductile metals. The gate electrode was made of Ti/Cr and the source-drain contacts of Al. The TFTs on Kapton have slightly higher off-current, lower on-current and lower mobilities than the same structure on glass. Nevertheless, the peak mobility for $V_{ds} = 10$ V is ~ 0.71 cm^2/Vs, suggesting that high-quality a-Si:H TFTs can be made with further process improvement.

3.1.2.2 Amorphous silicon TFTs on steel foil

As-rolled 1-μm to 25-μm thick 304 stainless steel foil serves as the substrate. Planarization with 0.5 μm thick spin-on glass removes the short-wavelength roughness of 0.3μm. This planarization, necessary for high transistor yield, functions as primary insulation. Further insulation is provided by a 0.5 μm thick plasma-enhanced CVD SiN layer. The TFTs are made in the inverted-staggered, back-channel etch configuration with 120 nm thick Cr gates, 320 nm PECVD gate SiN dielectric, 160 nm a-Si:H channel, and 50 nm n^+ a-Si contacts, followed by 120 nm Cr source/drain contacts. SiN and a-Si growth temperatures typically are 300°C and 250°C, respectively. A schematic cross-section of the TFT structure on the steel foil is shown in Figure 24. [6-10]

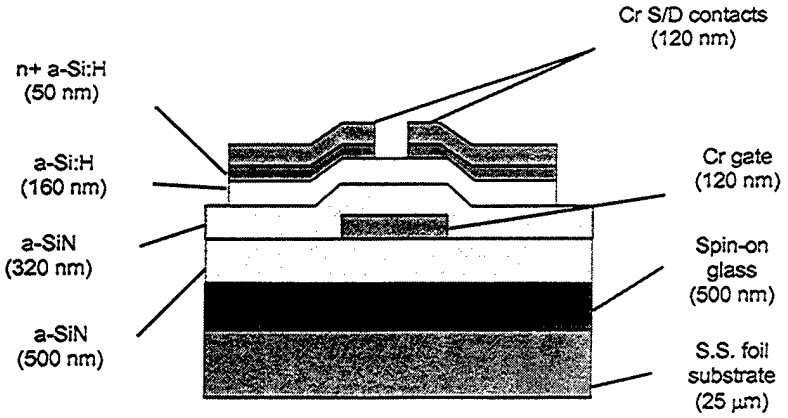


Figure 24. Cross-sectional schematic of a-Si TFT on planarized substrate of stainless steel foil.

3.1.2.3 Polycrystalline silicon TFTs on steel foil

The entire sequence of experiments for making transistors is represented in the overview of Figure 25. We start with as-received steel foil, planarize it and coat it with a diffusion barrier. A precursor layer of a-Si:H is deposited and then crystallized. From the polycrystalline silicon film, transistors are made in several configurations and by several processes. Not depicted in Figure 25 is the fabrication of integrated circuits.

We developed the substrate material and the device fabrication progressively in many increments of temperature. Initially it was not clear to which temperature the polysilicon-on-steel can be exposed. Therefore we report some of our earlier processing conditions as well as the more recent approaches. [11-13]

Substrate Preparation

200 μm thick foil of AISI grade 304 stainless steel (Fe/Cr/Ni 72/18/10 wt.%) was cleaned with acetone and methanol. To reduce the roughness of the steel foil surface, a 210 nm thick planarizing film of spin-on glass was applied to both sides and baked. Then a 270-nm thick film of SiO_2 was deposited on both sides by plasma-enhanced chemical vapor deposition (PECVD) at a substrate temperature of 250°C. The planarized and encapsulated substrate was heated in a tube furnace from 450°C to 800°C at a rate of 5°C/min. The ~0.5μm thick insulation layer reduced the RMS surface roughness from 5 nm for bare steel foil to <2 nm.

Deposition and crystallization of hydrogenated amorphous silicon

A 160 nm thick precursor film of a-Si:H was deposited by PECVD at a substrate temperature of 150°C. In TFT-on-glass technology, 600°C is the maximum crystallization and process temperature imposed by the softening of glass substrates. Raising the crystallization temperature raises both the crystal nucleation rate and the crystal growth rate exponentially, and correspondingly shortens the crystallization time. Because the rate of nucleation has a higher activation energy than the rate of crystal growth, raising the crystallization temperature above 600°C first increases the number of nuclei, reduces their size, and thus reduces the field effect mobility. Between 600°C and 800°C the nucleation rate keeps increasing faster with rising temperature than the growth rate. However, above some temperature the rate of nucleation begins to drop because the size of the critical nucleus grows. This is our rationale for exploring a wide regime of crystallization temperature. The nucleation rate is expected to drop at temperatures somewhere above 850°C while the growth rate keeps rising, so that at still higher temperature the grain size and hence the field effect mobility are expected to rise again. We explored crystallization temperatures up to 950°C.

Low temperature crystallization

We first exposed the a-Si:H precursor film for 1 hour to a hydrogen glow discharge to reduce the crystallization time by reducing the incubation time. [14] These seeded films then were crystallized at one of four different annealing temperature/time combinations: (a) 600°C for 6 hours; (b) 650°C for 1 hour; (c) 700°C for 10 minutes; and (d) 750°C for 2 minutes. These crystallization times were set assuming an activation energy of 2.7 eV for crystal growth in the a-Si: H precursor films, after exposure to the hydrogen discharge for pre-seeding. For

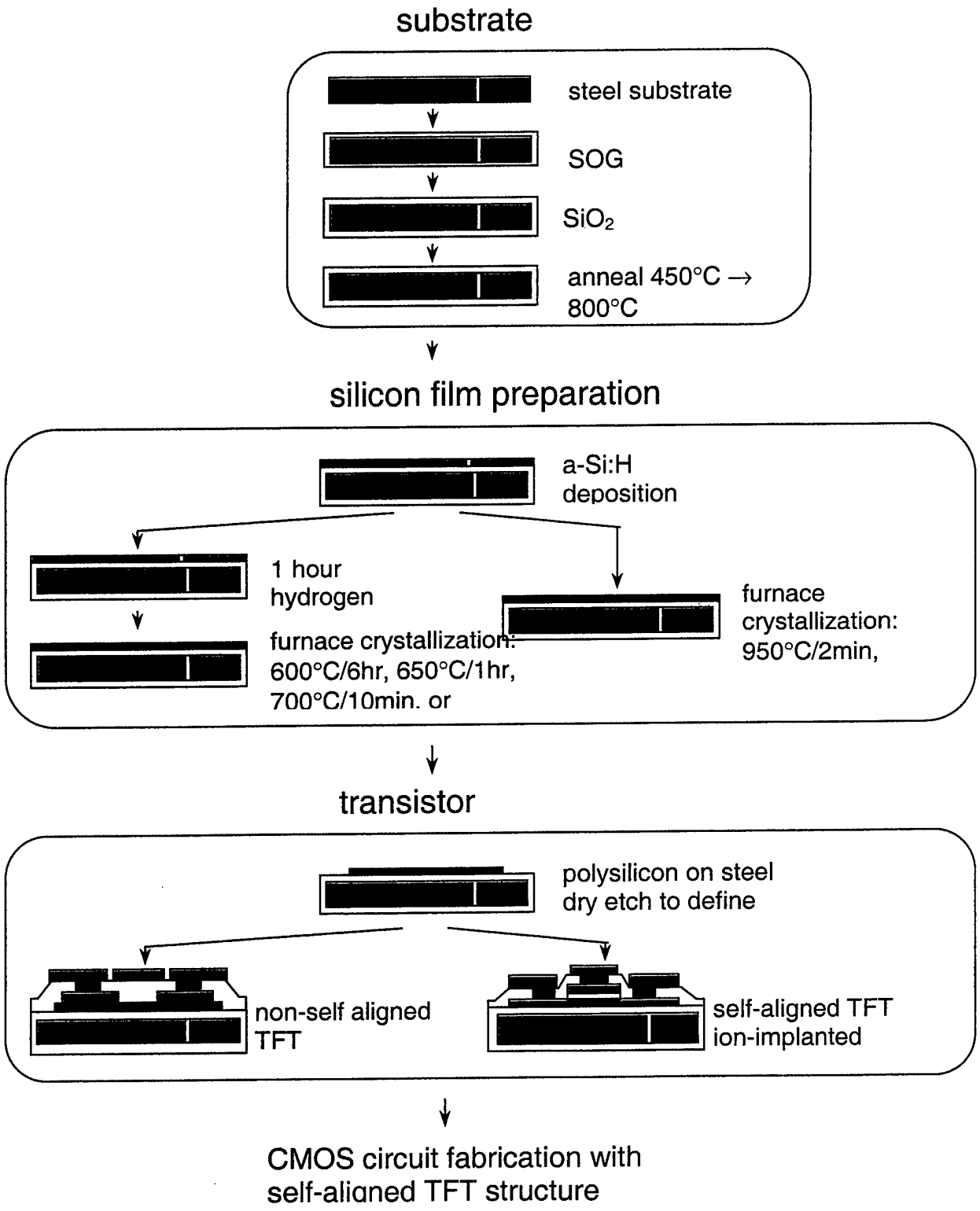


Figure 25. Overview of polycrystalline Si TFT processes on steel foil.

crystallization, first the hydrogen was driven out by heating in the 400°C zone of the furnace in flowing semiconductor grade N_2 gas for protection. Then the film was transferred to the center zone with the temperature set for crystallization. The transfer time and temperature ramping time were measured with a thermocouple to be less than 1 second. Progress and completion of crystallization were monitored *ex situ* by measuring the ultraviolet reflectance at $\lambda = 276$ nm.

The crystallization time of a-Si:H films without hydrogen plasma treatment drops faster with increasing temperature than that of hydrogen-plasma-treated films. This observation is consistent with a higher activation energy of nucleation in non-treated a-Si:H. We did not measure crystallization times, but in a separate test annealed an a-Si:H film that had not been hydrogen plasma treated at 750°C, also for 2 minutes (condition (d) of the samples listed above). UV reflectance at 276 nm indicated complete crystallization. This result suggests that seeding loses its importance as the crystallization temperature is raised above 600°C.

High temperature crystallization

The a-Si:H precursor films for crystallization at 950°C were not hydrogen plasma treated. These films were heated in the 400°C zone of the furnace, transferred to the 950°C zone and heated there for either 20 seconds or 20 minutes, in flowing nitrogen gas, and then cooled in the ~500°C zone. UV reflectance indicated complete crystallization. A transmission electron micrograph of such a polysilicon film crystallized at 950°C/20 sec. Shows an average grain size of ~0.5 μm.

The conductivities σ (in the dark) of all polysilicon films were measured at room temperature to check for possible doping by contamination from the metal substrate. They lie at $\sim 10^{-6}$ $S \cdot cm^{-1}$, i.e., not much above the conductivity of intrinsic polysilicon films prepared on glass substrates. The thermal activation energies are 0.53 eV and 0.72 eV for polysilicon and a-Si:H films, respectively. The activation energy of 0.53 eV suggests that the silicon grains are fully depleted.

Fabrication of polycrystalline silicon thin film transistors on steel foil

We made all transistors in the top-gate coplanar source/drain geometry. Initially we used a low-temperature device fabrication process with deposited source and drain layers. Once the high temperature capability of the polysilicon-on-steel had been ascertained, we moved to a high temperature process with ion-implanted source and drain. Replacing the deposited SiO_2 with a thermal SiO_2 came as the next step in the development of a high temperature process sequence.

Low temperature process: non-self-aligned structure with deposited source/drain

Because we wanted our initial TFTs to gauge the quality of the polysilicon films after the crystallization process, we started out by conducting all post-crystallization processing at low temperature. Thus we began by using a non-self-aligned process with a maximum process temperature of 350°C, instead of the conventional self-aligned process, which requires a post-implantation anneal at ~600°C. On top of the crystallized silicon film, a 75-nm thick n^+ (phosphorus doped) microcrystalline silicon (μc-Si:H) layer was deposited by PECVD at 350°C

to serve as the eventual source/drain. Then the original polysilicon layer was patterned into TFT islands by reactive ion etching (RIE), and the n^+ μc-Si:H layer was patterned by another RIE step. Next, a 200-nm thick gate oxide was deposited by PECVD at 250°C, followed by a wet etch to open the source/drain contact windows. 200 nm aluminum was thermally evaporated and then patterned by wet etch to form the gate and source/drain contacts. The final step in the TFT fabrication was a 15-minute-long anneal at 250°C in forming gas (15 vol.% hydrogen – 85 vol.% nitrogen). This source/drain process is not practical for short-channel TFTs, which require low parasitic resistance, but it is sufficient for evaluating the carrier mobility in long channels.

High temperature process: self-aligned structure with ion-implanted source/drain

The precursor a-Si:H film was crystallized and the active area defined by RIE. Next 150-nm gate SiO_2 was deposited by PECVD at either 250°C or 350°C, followed by the deposition of 200 nm intrinsic a-Si:H by PECVD at 270°C, which was then patterned by RIE to form the eventual gate. The SiO_2 layer was wet etched to form the source and drain openings. For n-channel TFTs, the source and drain were implanted with phosphorus at 50 keV and a dose of $2x10^{15}$ cm^{-2}. The implant damage was annealed out and the gate silicon was crystallized by a 30-minute furnace anneal at 750°C. Then the sample was immersed in a hydrogen glow discharge at 350°C for 1 hour. A 200-nm SiO_2 passivation layer was PECVD deposited at 250°C, and source/drain and gate contact windows were opened by wet etch of the passivation SiO_2. 300 nm Al was thermally evaporated and patterned to form the source/drain and gate electrodes. Finally, the TFTs were annealed in forming gas at 250°C for 15 minutes. The highest process temperature after crystallization was the 750°C post ion-implant anneal.

Self-aligned polysilicon TFT on steel with thermal gate oxide

The ability to crystallize device-grade films at 950°C suggested that the gate dielectric might be grown by direct oxidation of the polysilicon films, instead of PECVD. Polysilicon was formed by 950°C/20 sec crystallization and then individual TFT islands were defined by reactive ion etching (RIE). The polysilicon was oxidized in flowing dry O_2 for 40 minutes at 950°C in a tube furnace. The oxidation was followed by a 20-minute N_2 anneal at the same temperature, and then a 30-minute N_2 anneal at ~ 500°C. A lightly doped silicon wafer with [111] orientation was oxidized with the same process. The resulting oxide thickness was measured with a Dektak surface profiler and by ellipsometry to be 51 nm. The dielectric breakdown electric field of this thermal oxide was $4x10^6$ $V \cdot cm^{-1}$ and its leakage current density was ~$2x10^{-9}$ $A \cdot cm^{-2}$ under 15 V bias. To check for possible contamination introduced from the steel substrate during the oxidation process, a separate polysilicon film was annealed in N_2 for 40 minutes at 950°C. Its conductivity was ~ $3x10^{-6}$ $S \cdot cm^{-1}$. Because this is the same value as that of the 20-sec annealed polysilicon film, we concluded that the exposure to high temperature associated with thermal oxidation did not introduce dopants from the substrate into the polysilicon film.

Polysilicon TFT CMOS circuits on steel

To explore the eventual feasibility of polysilicon driver circuits on flexible substrates, Complementary Metal-Oxide-Semiconductor (CMOS) polysilicon circuits were fabricated on steel with a 6-mask process and tested. One mask is shown in Figure 26; the process, Figure 27. It includes individual n- and p-channel TFTs with two geometries and a range of channel dimensions, CMOS inverters, 5-stage ring oscillators, shift registers, and test patterns. The smallest gate length is 1 μm; the masks were written at the Penn St. Nanofabrication Facility. 150 nm a-Si:H was deposited by PECVD at 150°C and crystallized at 750°C/2 min. Islands were defined by RIE. The 150 nm SiO_2 gate dielectric was deposited by PECVD at 350°C, followed by 200 nm of a-Si:H deposited at 270°C for the gate. The a-Si:H and SiO_2 were patterned by RIE. After we deposited 200 nm SiO_2 as gate insulator, we patterned the SiO_2 gate and opened contact holes to the *n* and *p* channel TFT source and drain using BOE. Then we thermally evaporated Al, and patterned the Al using a wet-etch to form the gate, source and drain electrodes of the *n* and *p* channel TFTs, as well as the metal interconnects between the two gates, and the two drains of the *p* TFT and the *n* TFT.

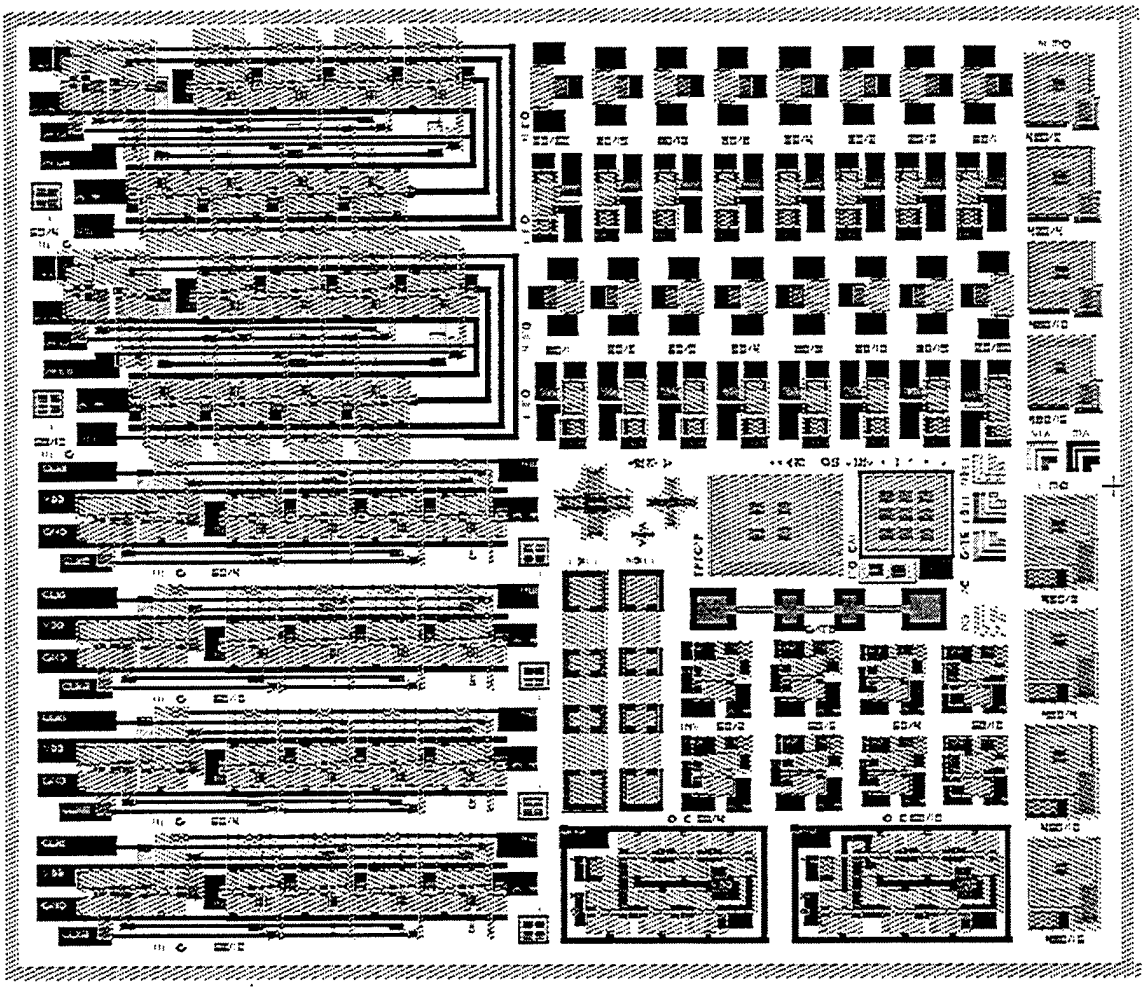


Figure 26. 4 x 4 mm die of the mask set for polysilicon TFT CMOS test

nc-Si TFT 150°C process

The devices are fabricated in a staggered top-gate, bottom-source/drain geometry which is adapted to the evolution of the nc-Si:H structure throughout its layer thickness.

The fabrication steps are shown in Figure 28. [19] The bottom nc-Si:H layer, which nucleates amorphous at its interface with a glass substrate, serves to develop crystallinity. The channel-layer proper is grown atop this nc-Si:H seed layer and the doped nc-Si:H contact layers. It is crystalline throughout and offers low resistance to the channel current, which is injected from the doped source layer into the undoped nc-Si:H channel layer, crosses its thickness, flows along the channel layer/SiO_2 interface, and again flows through the thickness of the channel layer into the doped drain layer. Addition of chlorine during the nc-Si:H growth makes the channel layer intrinsic instead of normally n-type, and thus reduces the barrier to hole injection. Inspection of the fabrication steps of Figure 28 shows that the active channel is formed precisely in the last-to-grow nc-Si:H layer. This ability to accurately position the active channel confers a considerable advantage over the coplanar top-gate structure, where the plasma etch for source/drain separation easily over-etches into the channel material.

The 230-nm intrinsic nc-Si:H seed layer is grown by 80-MHz excited plasma- enhanced chemical vapor deposition from SiH_4, H_2 and SiH_2Cl_2 on a glass substrate at 150°C. On it is evaporated 50-nm thick Cr as the source/drain-contact metal, and the 60-nm p^+ (or n^+) nc-Si:H is grown by VHF PECVD. This contact bi-layer is patterned by plasma etching to define source and drain. The intrinsic nc-Si:H channel layers are deposited at a pressure of 500 mtorr, absorbed power of 86 mW/cm^2 to 93 mW/cm^2, and a substrate temperature of 150°C. At the hydrogen-dilution ratio of $R = [H_2]/[SiH_4+SiCl_2H_2] = 20$ to 30, the two bands in the ultraviolet-reflectance spectrum at $\lambda = 276$ nm and 365 nm indicate that the film is crystalline whether deposited over the nc-Si:H seed layer or over the doped layer on Cr. Addition of dichlorosilane reduces the electrical dark conductivity at room temperature to ~ 6×10^{-7} S·cm^{-1} for R = 20, and ~ 3×10^{-6} S·cm^{-1} for R = 30. For gate insulator we use 235-nm thick electron-cyclotron-resonance SiO_2 grown at 140°C, or 370-nm thick PECVD SiO_2 grown at 150°C. After opening the contact holes by wet chemical etching, 200-nm Al is thermally evaporated for contacts, and is patterned. The maximum process temperature for n-channel structures is 150°C. For p-channel TFTs all process temperatures are 150°C or less, except for the p^+-layer deposition temperature, which we set to either 150°C or 280°C on account of the difficult p^+ doping of nc-Si:H at low temperature. In our opinion, p-type doping and charge trapping in the interface and insulator pose the biggest challenges to developing a practical device technology.

Evaluation of electrical response to mechanical deformation

We introduced compressive strain to individual transistors by inward cylindrical bending. In most cases the bending direction was perpendicular to the gate, as shown by arrows in Figure 29. In this bending configuration we used two types of probes, 'soft' and 'hard', for measuring the transfer characteristics. A few TFTs were also tested under bending direction parallel to the gate using 'soft' probes. Single TFTs were bent to different radii of curvature *R*, ranging from 70 to 1.6 mm. Some TFTs were measured repeatedly at different *R*, others were permanently bent to a fixed *R* to monitor the change in the transfer characteristics for ~ 40 hours.

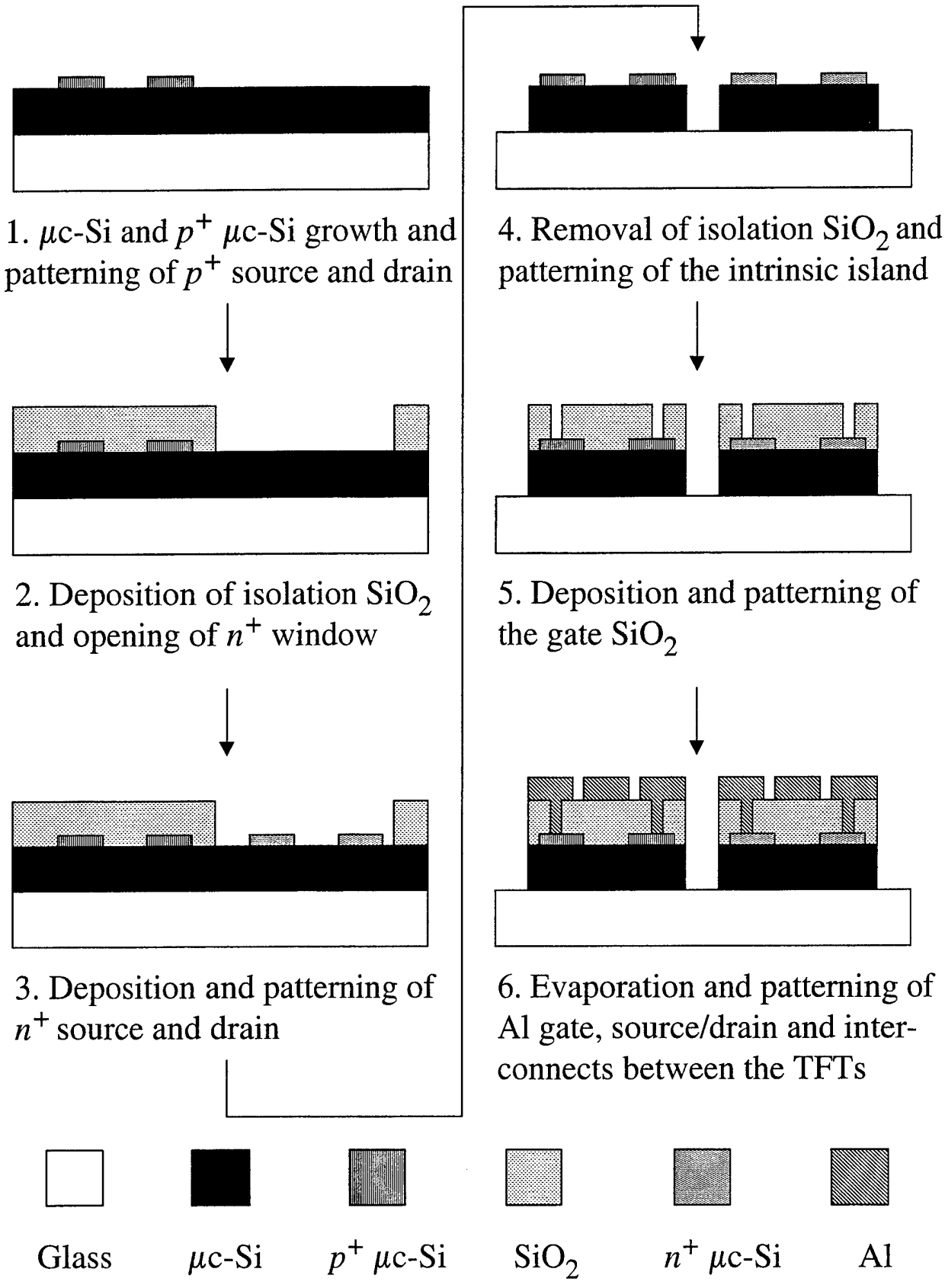


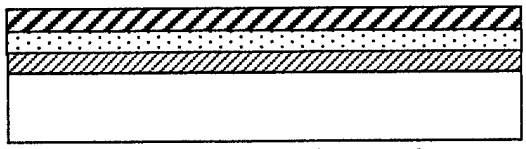
Figure 27. CMOS process using TFTs made from nanocrystalline silicon.

We describe the nc-Si CMOS process with Figure 28. [14-19] Both the *p* type and the *n* type TFT use one single directly deposited μc-Si layer as the conducting channel. The nc-Si channel material is grown by plasma-enhanced chemical vapor deposition (PECVD) in a process similar to the deposition of a-Si:H. The undoped channel and the p^+ and n^+ contact layers were grown by PECVD in two separate (*i* layer / doping) chambers. The SiO_2 gate dielectric also was grown by PECVD but in a different system. The channel layers of undoped *i* nc-Si were grown on Corning 7059 glass, by DC excitation of a mixture of SiH_4, SiF_4 and H_2. X-ray diffraction and Raman scattering, and an electron mobility of 4.9 cm^2/Vs in separately made *n* channel TFTs prove that the films are microcrystalline. Adding SiF_4 to the source gas changes the growth chemistry, provides a wider range of structure, and a lower growth temperature than deposition from H_2-diluted SiH_4 alone. *n* channel TFTs of nc-Si grown with SiF_4 have exhibited the highest electron mobility reported to date. The growth rate was 0.6 Å/s at a power density of 160 mW/cm^2. The dark conductivity of the *i* nc-Si is 1 x 10^{-7} S/cm, and its thermal activation energy is 0.55 eV. The p^+ and n^+ source/drain contact layers were grown from SiH_4, H_2, and B_2H_6 or PH_3 by RF excitation at 13.56 MHz. Their dark conductivities are 0.01 S/cm (p^+ nc-Si) and 20 S/cm (n^+ nc-Si).

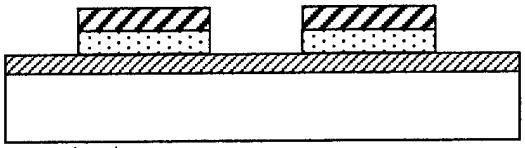
The TFTs were made in the top-gate configuration shown in Figure 28. The CMOS inverter is made of a *p* channel TFT and an *n* channel TFT of identical structure. A six-level mask process with specially designed masks was used in the inverter fabrication. First, 300 nm of *i* nc-Si and 60 nm of p^+ nc-Si layer were grown on the substrate without breaking vacuum. Next, we patterned the p^+ nc-Si source and drain for the *p* channel TFT using reactive ion etching (RIE) with 10% O_2 and 90% CCl_2F_2. Deposition of 200-nm layer of isolation SiO_2 followed. Then we opened a window in the SiO_2 using buffered oxide etch (BOE) to deposit a 60 nm n^+ μc-Si layer. After RIE patterning of the n^+ nc-Si source and drain for the *n* channel TFT, we removed the SiO_2 layer with BOE, and followed by the definition of the *i* nc-Si island using RIE. The channel nc-Si now exposed was oxidized for 10 minutes in 1:3 H_2O_2 : H_2SO_4 , then dipped for 10 seconds in BOE, rinsed in deionized water, blow-dried in nitrogen, and immediately introduced into the system for gate insulator deposition.

From each set of transfer characteristics we extracted the off-current I_{off}, on-current I_{on}, gate leakage current I_{leak}, linear mobility μ, threshold voltage V_{th}, and subthreshold slope *S*. The definition of these currents is as follows: the off-current is the smallest drain-to-source current at V_{ds} = 10V, the on-current is the drain-to-source current for V_{ds} = 10 V and $V_{gs} = V_{th}$ + 10 V, and the leakage current is the gate-to-source current for V_{ds} = 10 V and V_{gs} = 20 V. V_{th} and μ were calculated from the transfer characteristic for V_{ds} = 0.1 V using the metal-oxide-semiconductor field-effect transistors (MOSFET) equations for the linear regime, while *S* was obtained by fitting an exponential function in the subthreshold region of the transfer characteristic for V_{ds} = 10 V. To obtain reference values for these parameters, each TFT was measured before any compressive strain was applied. We calculated the compressive strain at the SiN_x/a-Si:H interface of the TFTs assuming that the Young's moduli of our polyimide substrate and the TFT layers are 5 GPa and 183 GPa, respectively. The highest strain, at the smallest bending radius *R* = 1.6 mm, was ~ 1%. [20-25]

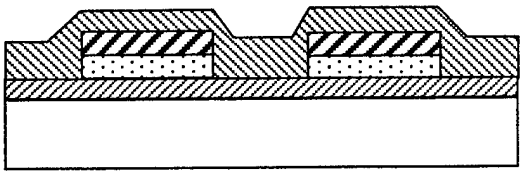
1. 230nm nc-Si buffer/seed layer deposition on Corning 1737 glass at 150°C



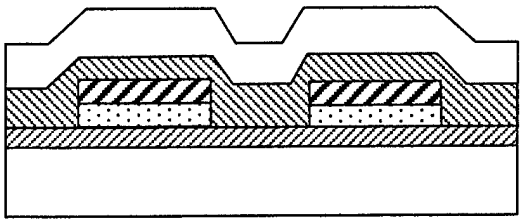
2. 50nm Cr evaporation and 60nm p^+/n^+ nc-Si deposition at 150°C or 280°C



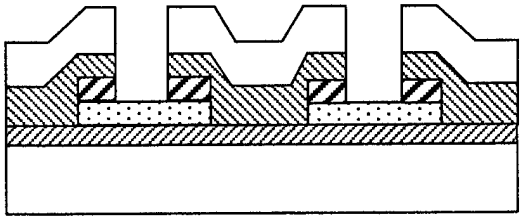
3. p^+/n^+ nc-Si & Cr patterning as source/drain



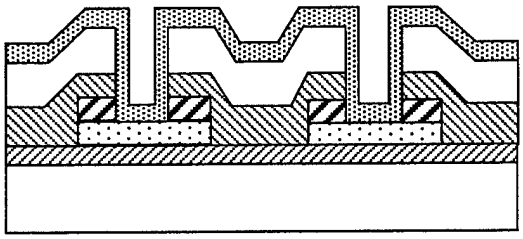
4. 50nm intrinsic nc-Si channel layer deposition at 150°C



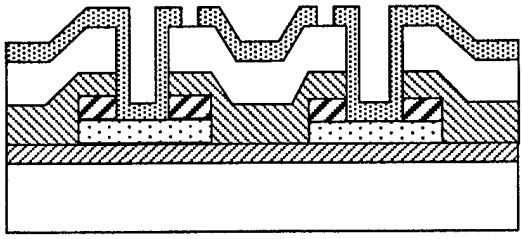
5. ~300nm ECR or PECVD gate-SiO_2 at 140°C or 150°C



6. Contact hole patterning



7. 200nm Al evaporation



8. Al gate & source/drain contact patterning

Figure 28. Process sequence for fabricating nc-Si TFTs in the staggered geometry.

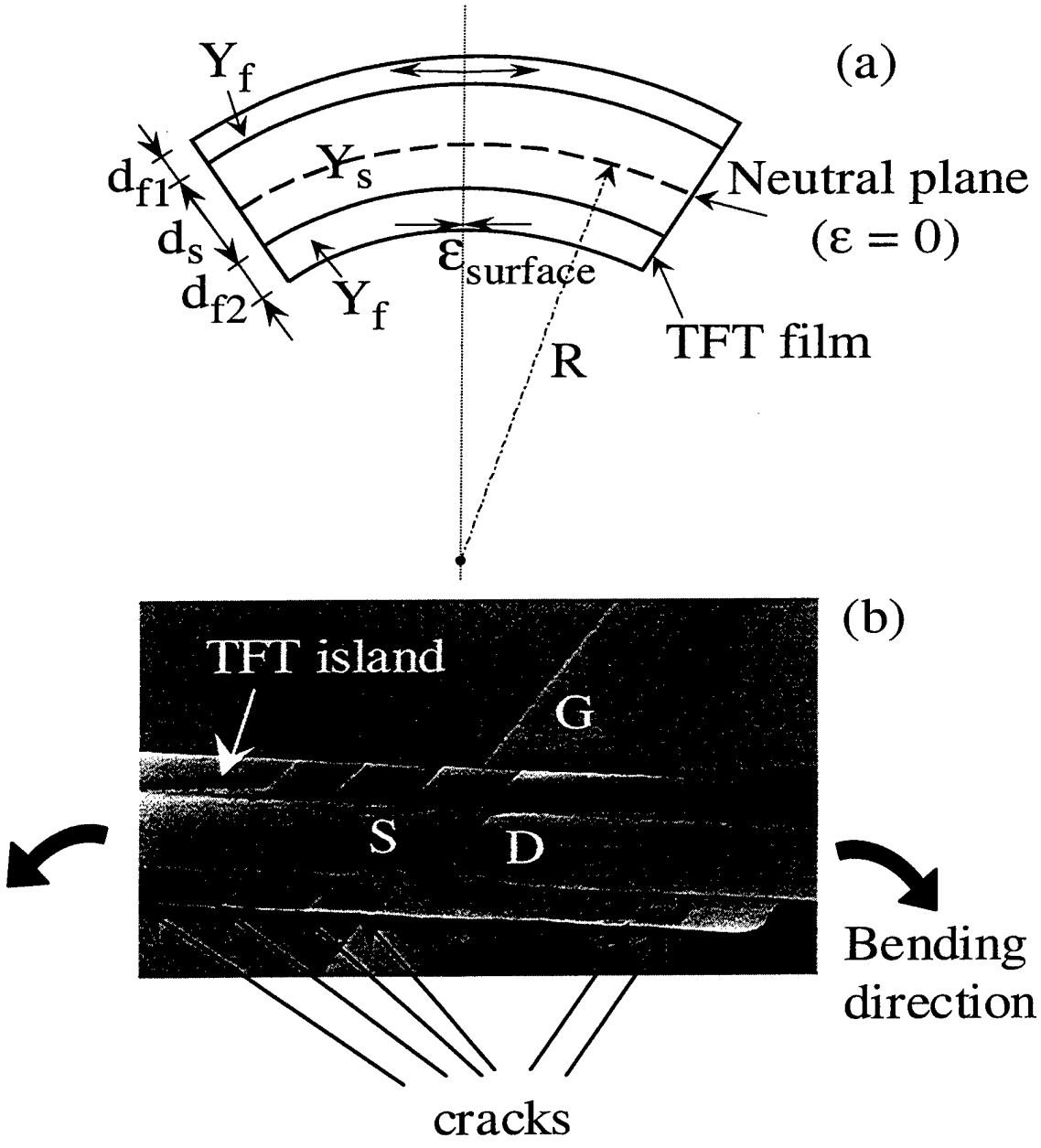


Figure 29 (a) Geometry of a bent TFT film-on-foil structure. (b) SEM micrograph of a TFT on Kapton that fractured under tensile (outward) bending, as indicated by the arrows.

RESULTS AND DISCUSSION

Amorphous silicon TFTs on Kapton foil

The key electrical properties of the TFTs are reflected in the transfer characteristics. These are plotted in Figure 30. for drain-to-source voltages V_{ds} = 0.1 V and 10 V. At V_{ds} = 10 V, the off-current is ~ 2 x 10^{-12} A (~ 5 x 10^{-14} A/μm of gate width) and the on-off current ratio is ~ 10^{7}.

Another important way of representing the measured transistor performance is shown in Figures 31 (a) and (b). The drain-to-source current I_{ds} and its square root are plotted as a function of gate-to-source voltage V_{gs} for the TFT of Figure 30. These plots are used to determine the threshold voltage V_T and the electron field-effect mobility μ_n in the linear and the saturation regime, using the following equations originally derived for MOSFET on crystalline silicon:

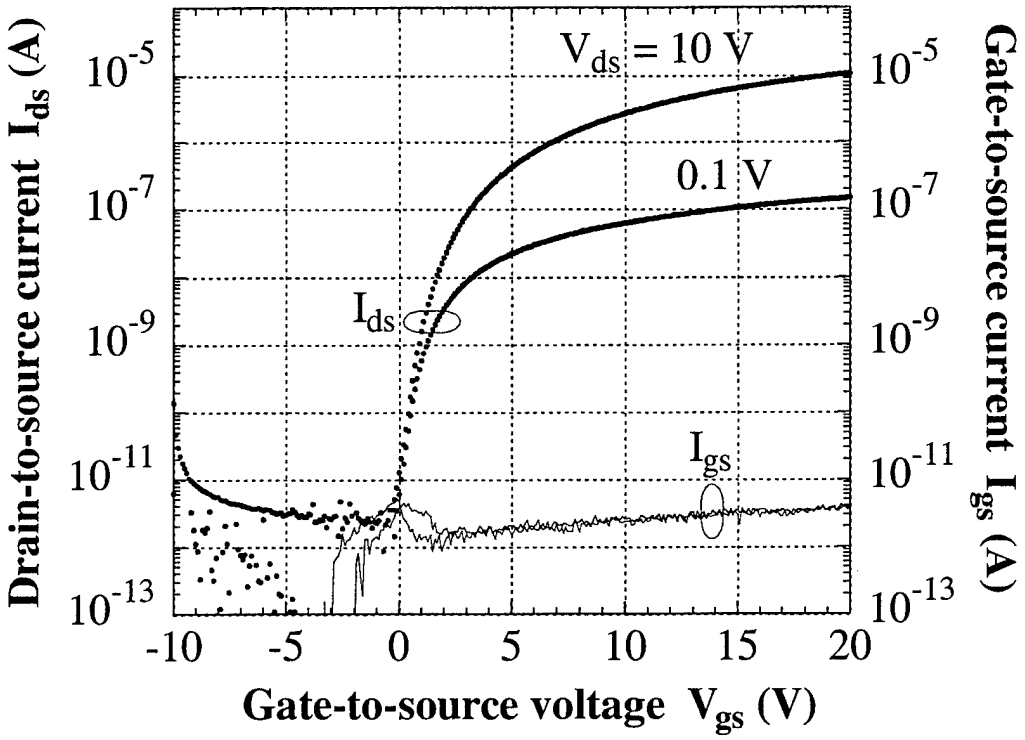


Figure 30. Transfer characteristics of a typical a-Si TFT made at 150°C on Kapton foil.

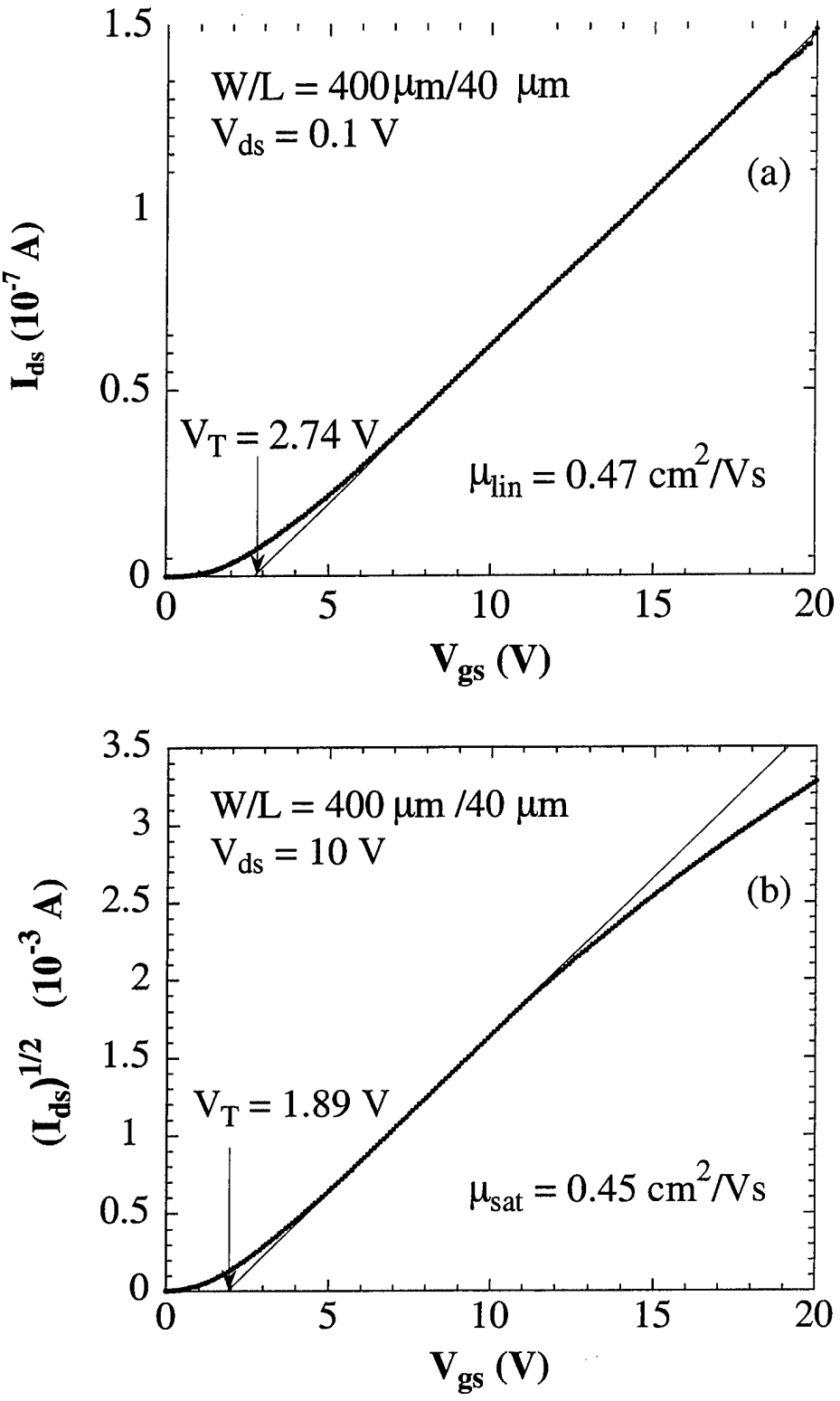


Figure 31. Extraction of (a) linear and (b) saturated mobility from the data of Figure 30.

$$I_{ds(linear)} = \mu_n C_{SiN} \frac{W}{L}\left[\left(V_{gs} - V_T\right) V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad \text{(small } V_{ds}\text{)}$$

$$I_{ds(saturated)} = \mu_n C_{SiN} \frac{W}{2L}\left(V_{gs} - V_T\right)^2 \qquad \text{(large } V_{ds}\text{)}$$

where C_{SiN} is the capacitance of the gate insulator, W the channel width, and L the channel length. The dielectric constant of our 150°C silicon nitride is 7.4 and we calculate C_{SiN} = 1.82 x 10^{-8} F cm^{-2}. In the linear regime we obtain V_T = 2.84 V and a mobility of 0.47 cm^{2}V^{-1}s^{-1}. At V_{ds} = 10 V we obtain V_T = 1.89 V and a saturated mobility of 0.45 cm^{2}V^{-1}s^{-1}, and a subthreshold slope $S = dV_{gs}/d(\log I_{ds})$ of ~ 0.5 V/decade. These values demonstrate that good quality a-Si:H TFTs can be fabricated on thin foils of polyimide.

Thus, we fabricated good quality amorphous silicon thin-film transistors on an organic polymer foil at the maximum process temperature of 150°C. In the TFT fabrication, each layer is optimized for the best electrical performance and low built-in mechanical stress. Therefore, the foil is flat after TFT fabrication. The off-current is ~ 2 x 10^{-12} A, the on-off current ratio ~ 10^7, the threshold voltage ~ 2V, the mobility ~ 0.5 cm^2/Vs, and the subthreshold slope ~ 0.5 V/decade.

Amorphous silicon TFTs on steel foil

All but the 1-μm substrate produced functional transistors. Typical TFT performance metrics are presented in summary form in Figure 31. Results vary with substrate thickness. For the most part, this is indeed evident from Figure 32. Slight variations of certain metrics do occur, however, for the thickest and thinnest substrates. The higher threshold voltage (V_T) values for devices on the 200-μm and 75-μm substrates are a result of deeper back-channel over-etch, which brings any positive charge on the back-channel closer to the accumulation layer and thus raises V_{TH}. Since this deeper over-etch reduces the thickness of the i-layer in the n-channel region, it should also reduce I_{OFF}, which is confirmed by the data. The slight drop in TFT performance observed for devices on the 3 μm thick foil, however, is a result of our lack of experience in the handling of such thin foils rather than device physics. Yet, the ability to obtain functioning TFTs on substrates as thin as 3 μm is remarkable: this substrate is not even three times as thick as the 1.2-μm structure that was grown on it is not actively involved in the operation of the device, the TFT metrics are not expected

This ruggedness of thinner substrates can be explained by examining the force balance equations describing the coupling of two layers such as a thin deposited film and a substrate. When the film-substrate couple is strained, the distribution of stress is such that the force (per unit width) in the film equals that in the substrate.

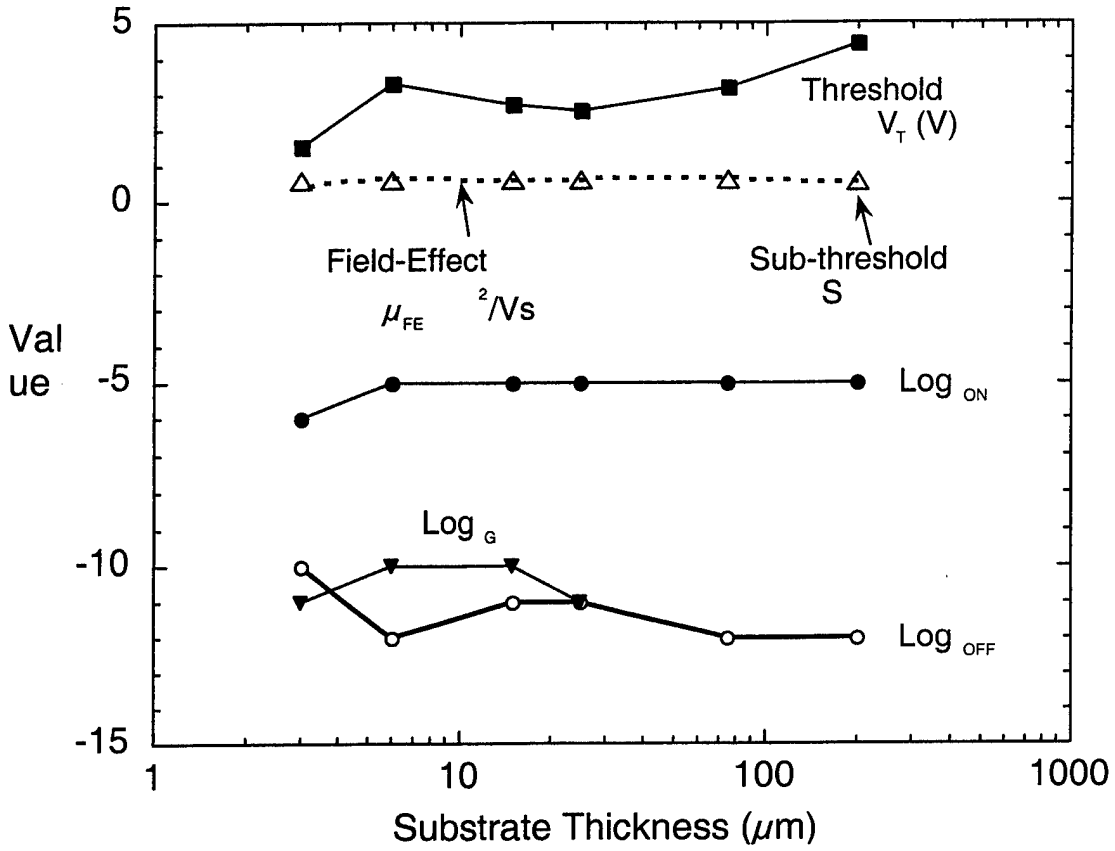


Figure 32. Summary of the TFT properties as a function of steel foil substrate thickness. I_{ON} and I_{OFF} are the ON and OFF source-drain currents, and I_G is the source-gate leakage current.

That is,

$$\sigma_f d_f = \sigma_s d_s$$

where $\sigma_{f,s}$ represent the stresses in the film and the substrate, and $d_{f,s}$ correspond to the film and substrate thickness. Using the stress-strain relationship, $\sigma = Y'\varepsilon$, where Y' is the biaxial modulus of elasticity and ε is the strain, the above equation can be expanded to:

$$Y'_f \varepsilon_f d_f = Y'_s \varepsilon_s d_s$$

Rearranging, we obtain the compliance relation,

$$\varepsilon_f / \varepsilon_s = (Y'_s d_s) / (Y'_f d_f)$$

which indicates that, for a given set of materials and a fixed film thickness, the strain in the film ε_f can be minimized by reducing the substrate thickness d_s. This is desirable for thin-film electronics where mechanical stress during and after fabrication may affect not only the electrical

performance of devices but also the mechanical integrity of the electronic layer itself, leading in some cases to cracking and peeling of films.

A fortuitous combination of material properties also helps stabilize a-Si:H TFTs on steel substrates. During fabrication of the TFTs, the substrates exhibited varying degrees of curvature, sometimes concave, other times convex, depending on the particular processing step. Remarkably, the finished structures were nearly flat. (When the substrate exhibited some initial curvature, there was little change in the degree of bending.) Since the films were deposited at elevated temperatures, measurement of substrate curvature at room temperature must reflect the effect of differential thermal contraction between the deposited film and the substrate. The fact that the final substrate curvature was very similar to the initial curvature indicates that the stress due to differential thermal contraction σ_{DTC} must be balanced by the intrinsic film stress σ_I:

$$\sigma_f = \sigma_{DTC} + \sigma_I \cong 0$$

From the radii of curvature, the biaxial moduli and thicknesses of films and substrate, and the process temperature, we calculate that $\sigma_I = 1.5$ GPa. The balance between σ_I and σ_{DTC} helps explain the surprising ruggedness of TFTs made on very thin steel foils.

Polycrystalline silicon TFTs on steel foil

The TFTs were evaluated while the steel foil was flat and kept grounded. Transfer characteristics (drain current I_{DS} against gate-source voltage V_{GS}) and output characteristics (drain current I_{DS} against drain-source voltage V_{DS}) were measured with an HP 4155 parameter analyzer to evaluate the device performance and material properties. The drain current ON/OFF ratio is defined as the ratio of highest drain current (ON current) to lowest drain current (OFF current) at $V_{DS} = 10$ V. The DC characteristics of the CMOS inverters were measured with the same HP 4155 parameter analyzer, and the transient characteristics of the CMOS inverters and ring oscillators were measured with a Tektronix 3200 digital oscilloscope using very low capacitance probes.

Non-self-aligned TFTs with deposited source/drain

These lowest-process-temperature TFTs were made from polysilicon crystallized at one of five temperature/time combinations: 600°C/6 hour, 650°C/1 hour, 700°C/10 min, 750°C/2 min, and 950°C/20 sec. Figure 33 shows the (a) transfer and (b) output characteristics of a transistor made from 650°C polysilicon. We calculated the threshold voltage V_{th} and the electron field effect mobility in the linear regime $\mu_{e,lin}$ from the linear plot of the drain current I_{DS} against gate source voltage V_{GS} at the drain-source voltage V_{DS} of 0.1 V. This transistor has $\mu_{e,lin} = 64$ $cm^2 \cdot V^{-1} s^{-1}$ and $V_{th} = 7$ V. The value of $\mu_{e,lin}$ lies among the highest of all transistors made from furnace-crystallized polysilicon. The I_{DS} ON/OFF ratio is ~10^6 over the entire range of 600°C to 950°C, a ratio comparable to those of transistors made on glass with the same process. This ratio suggests that TFT performance is not adversely affected by the high temperature crystallization of silicon on the steel substrates.

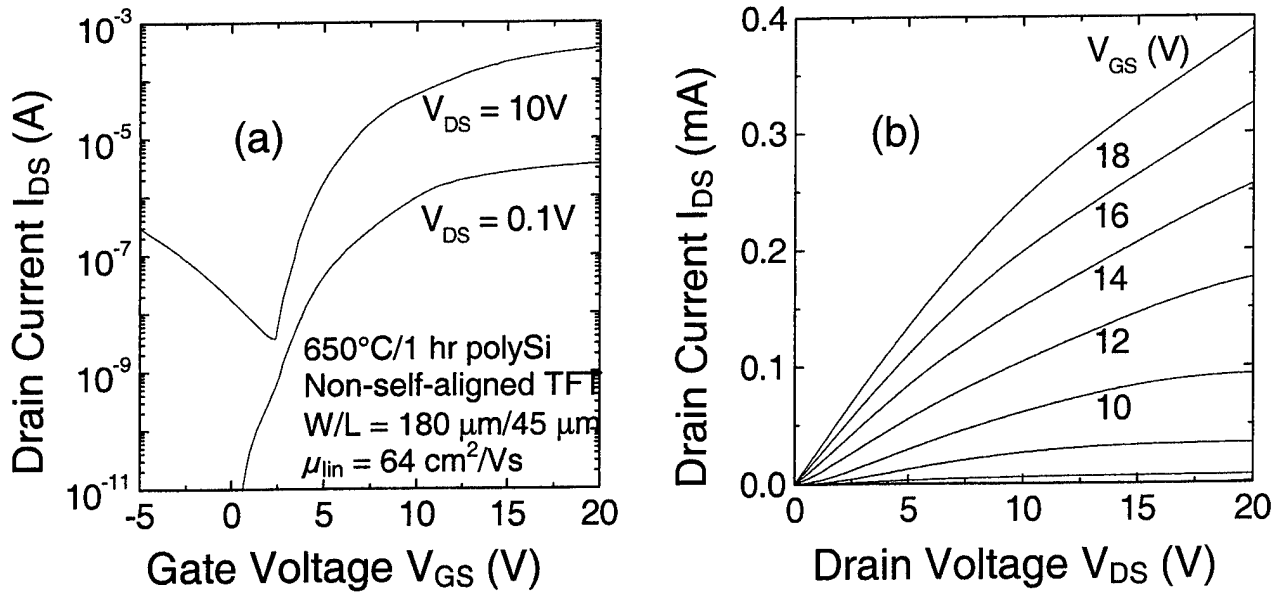


Figure 33. (a) Transfer characteristics and (b) output characteristics of a top-gate polysilicon TFT with deposited source/drain process. Polysilicon was made by crystallization at 650°C/1 hour on steel.

Self-aligned TFT with ion-implanted source/drain

Self-aligned TFTs were made of polysilicon crystallized at 950°C/20 sec or 950°C/20 min. TFTs made from 950°C/20 sec polysilicon and TFTs made from 950°C/20 min polysilicon, both with 250°C gate SiO_2, have electron mobilities $\mu_{e,lin}$ of 6 $cm^2 \cdot V^{-1}s^{-1}$ and 15 $cm^2 \cdot V^{-1}s^{-1}$ respectively. The higher $\mu_{e,lin}$ of the 20 min polysilicon TFT may be the result of the reduction of grain boundary defects by high temperature annealing. Figure 34 (a) shows the transfer characteristic of a TFT made from 950°C/20 min polysilicon but now with a 350°C gate SiO_2. The uniformly higher mobilities of the TFTs with 350°C gate SiO_2 for all TFT channel lengths, shown in Figure 34 (b), point to the importance of the quality of the gate dielectric and of its interface with the channel material. The transistors made with 20-min annealed polysilicon have the same OFF current as the transistors made with 20-sec annealed polysilicon. These results suggest again that the TFT performance is not adversely affected by metal contamination from the substrate.

Self-aligned TFT with thermal oxide

Taking advantage of the high temperature capability of steel substrates that we had proven at this point, we explored the possibility of transferring standard IC fabrication techniques to the polysilicon-on-steel process. This was the purpose of thermal oxidation of the polysilicon TFTs on steel to form the SiO_2 gate dielectric. A polysilicon TFT on steel with 51 nm-dry SiO_2 as gate dielectric, and a channel 5 μm long and 50 μm wide, has V_{th} = 8.5 V, $\mu_{e,lin}$ = 27 $cm^2 \cdot V^{-1}s^{-1}$ and $\mu_{e,sat}$ = 32 $cm^2 \cdot V^{-1}s^{-1}$, and the OFF current I_{DS} is 35 pA per μm of channel width at V_{DS} = 10V.

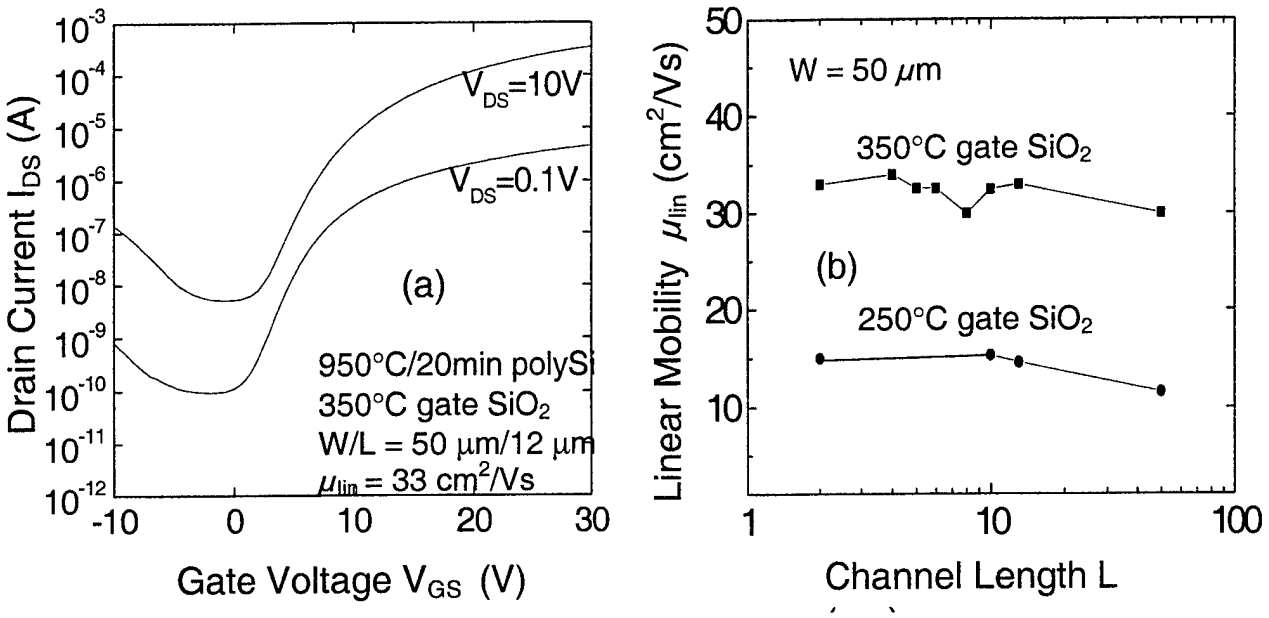


Figure 34. (a) The transfer characteristic of a self-aligned TFT made of 950°C/20 min polysilicon and 350°C gate SiO_2, and (b) mobility and OFF current vs. channel length for TFTs with gate SiO_2 deposited at 250°C and 350°C.

P-channel TFT with 950°C polysilicon and self-aligned process

One advantage of polysilicon over a-Si:H is its CMOS capability, which opens a wider range of applications, including circuits with low power consumption. In preparation for making CMOS circuits, we fabricated p-channel polysilicon TFTs using the self-aligned structure. The polysilicon was formed by furnace crystallization of 150°C a-Si:H at 950°C/20 sec, or 750°C/2 min. The gate dielectric was 150-nm 350°C PECVD SiO_2. A TFT made with 750°C/2 min polysilicon and a TFT made with 950°C/20 sec polysilicon have μ_{lin} = 22 $cm^2 \cdot V^{-1}s^{-1}$ and 14 $cm^2 \cdot V^{-1}s^{-1}$, respectively. The threshold voltages V_{th} of both TFTs are ~ -20 V.

Effects of TFT geometry: channel length, edge leakage

We studied two aspects of TFT geometry that can affect TFT performance. One aspect is the channel length L. The other is the edge leakage current. These studies were made on devices using the self-aligned process and deposited SiO_2, from polysilicon crystallized at 750°C/2 min. When L is less or comparable to the silicon grain size, the TFT channel may contain not even one grain boundary. The absence of the electrostatic barrier associated with the grain boundary enables a higher field mobility.

The edge leakage current was studied by comparing the electrical characteristics of the two types of TFTs, one whose drain surrounds the gate, and the other with a conventional open

gate. The result shows that edge leakage contributes to the OFF current, and points to the need for careful surface passivation.

Figure 35 contains a plot of the field effect mobility and the threshold voltage for p- and n-channel devices as a function of channel length, which ranges from 1 μm to 10 μm. The TFTs with channel lengths $L \leq 2$ μm show substantially better performance than the TFTs with longer channels, in particular the n-channel devices. This result suggests that the grain size in 750°C/2 min polysilicon may be as large as 2 μm or that one hour of post ion-implantation hydrogenation was not long enough for TFTs with channels ≥ 2 μm.

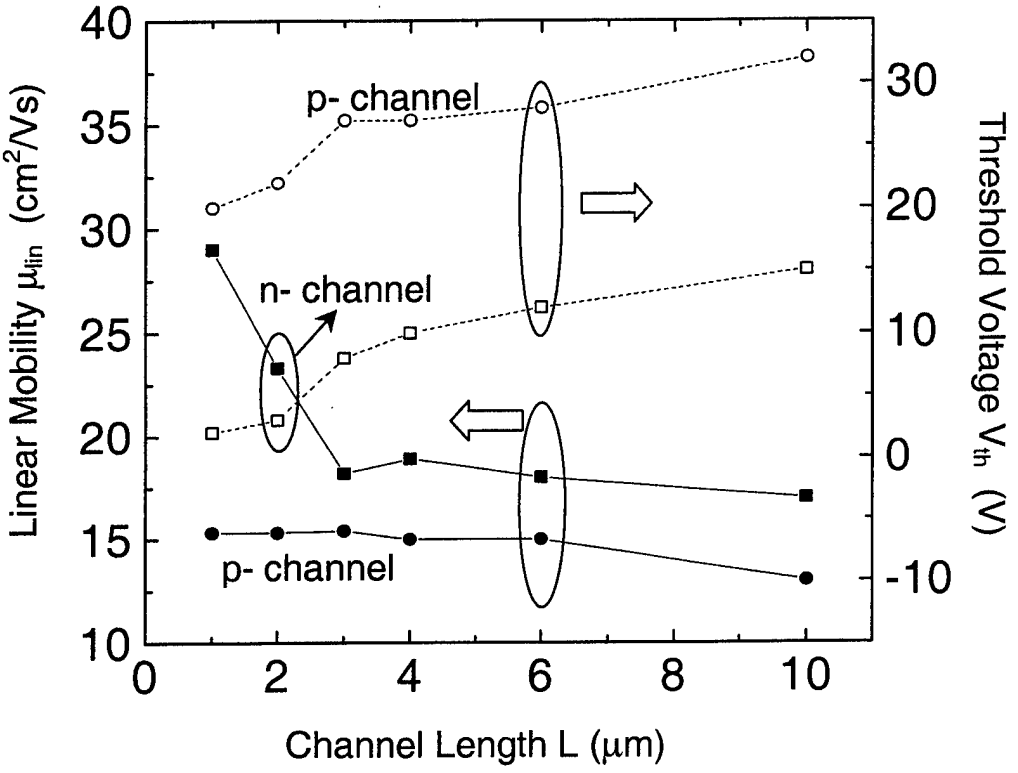


Figure 35. The linear mobilities and threshold voltages of open-end n- and p-channel TFTs plotted vs. channel length from 1 μm to 10 μm.

CMOS test circuits of polycrystalline silicon on steel foil

Figure 36 shows the DC output characteristics of a CMOS inverter made from polysilicon TFTs with channel length L = 6 μm and width W = 60 μm. Both the output voltage and the power are plotted on a linear scale against the input voltage. This inverter has a full range swing from the power supply voltage V_{DD} to ground. The output voltage gain K is defined as $\Delta V_{OUT}/\Delta V_{IN}$ at the threshold voltage. This inverter has a gain K of ~25 at $V_{DD} \geq 20V$. The threshold voltage is not exactly half of V_{DD} due to the difference between the n- and p-channel TFT threshold voltages.

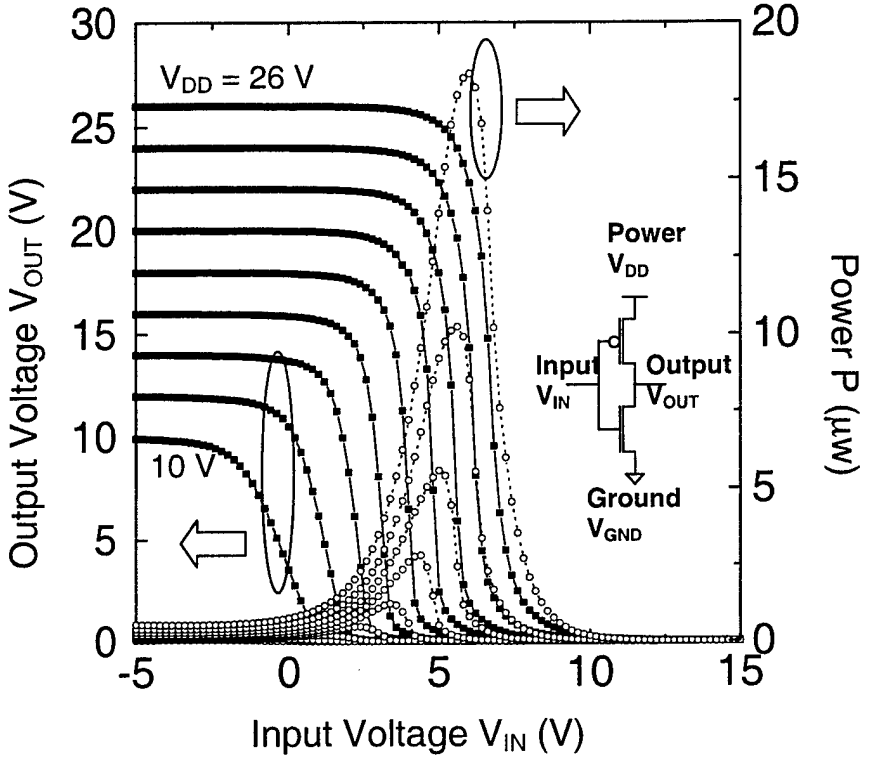


Figure 36. DC output characteristic of CMOS inverter made with polysilicon TFTs on steel with channel width W = 60 μm and length L = 6 μm.

The CMOS polysilicon inverter operates at 1 MHz with a power supply V_{DD} = 30 V and an input signal peak-peak amplitude of 22 V. The n- and p- channels have width W = 60 μm and length L = 2 μm. The RC time constants for the rise and fall phases are T_r = 190 ns and T_f = 130 ns respectively. These values are consistent with the calculated channel resistance R_{ch} of the transistor and the load capacitance C_{para}, which is the parasitic capacitance of the output contact pad to the steel substrate. The propagation delay in the rise phase is calculated with the following equations:

$$T_f = C_{para} \cdot R_{ch} = C_{para} \cdot V_{DS}/I_{ch}$$

$$I_{ch} = \mu_e \cdot (\varepsilon_{ox}\varepsilon_0/t_{ox,gate}) \cdot (V_{GS}-V_{n,th}) \cdot V_{DS}$$

$$R_{ch} = [\mu_e \cdot (\varepsilon_{ox}\varepsilon_0/t_{ox,gate}) \cdot (V_{GS}-V_{n,th})]^{-1}$$

$$C_{para} = [A_{D/S}/t_{ox,ins} + A_{metal}/(t_{ox,ins} + t_{ox,pass})] \cdot (\varepsilon_{ox}\varepsilon_0)$$

The load capacitance C_{para} = 0.96 pF is calculated from the geometry of the output pad. $A_{D/S}$ is the drain area of the pull-down and pull-up devices, i.e., the drains of the n-channel TFT and p-channel TFTs. A_{metal} is the metal pad area. $t_{ox,ins}$ and $t_{ox,pass}$ are the thicknesses of insulation SiO_2 (480 nm spin-on-glass and PECVD SiO_2 between the polysilicon and the steel substrate) and the passivation SiO_2 (200 nm PECVD SiO_2); using μ_{lin} = 20 $cm^2 \cdot V^{-1}s^{-1}$, ε_{ox} of SiO_2 =3.9, a gate SiO_2 thickness $t_{ox,gate}$ = 150 nm, V_{GS} = 18 V as the input HIGH voltage, $V_{n,th}$ = 3V for the n-channel threshold voltage, and R_{ch} = 1.7x10^5 Ω, the calculated value of the fall time $T_{f,calc}$ = 163ns. This is relatively close to the experimental value T_f = 130 ns.

Figure 37 shows (a) the AC signal of a 5-stage ring oscillator made with the CMOS polysilicon inverters and (b) the oscillation amplitude and frequency vs. the supply voltage. The TFTs have channel width W = 60 μm and length L = 4 μm. The oscillation frequency f_{osc} is 1.03 MHz and its amplitude A_{osc} is 7.1 V at a power supply voltage V_{DD} = 30 V. The oscillation frequency rises when the power supply voltage V_{DD} is raised above 15V, while the oscillation amplitude A_{osc} saturates at 7.1V.

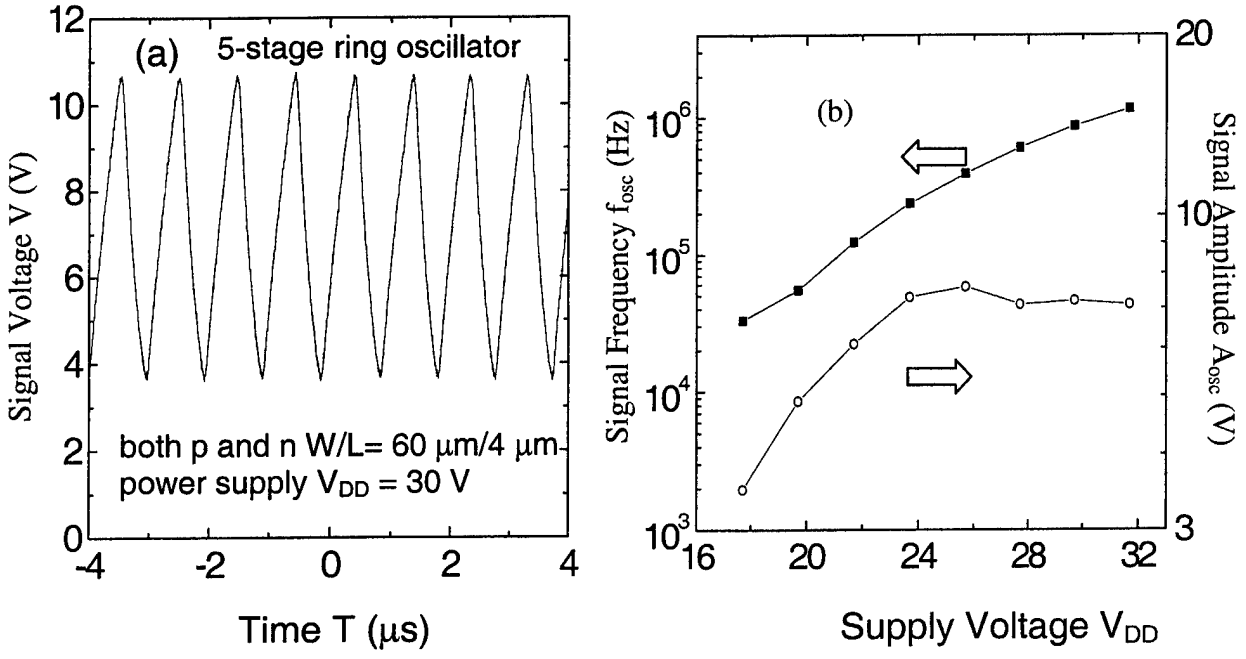


Figure 37. (a) AC output signal of a 5-stage ring oscillator made with CMOS polysilicon inverters on steel. TFTs have channel width W = 60 μm and length L = 4 μm.
(b) The oscillation amplitude and frequency plotted in log scale vs. the power supply voltage.

3.1.2.4 Nanocrystalline silicon TFTs

nc-Si TFTs and CMOS inverter made at 320°C

Figure 38 shows the transfer characteristics of the *p* channel and *n* channel TFTs of the inverter. We define the ON current I_{ON} as the drain current I_d at a gate voltage V_{gs} of (- or +) 25 V, and the OFF current I_{OFF} as the lowest drain current, both at a drain voltage of V_{ds} of (- or +) 10 V. Figure 38 (a) shows a *p channel TFT* ON/OFF current ratio of > 10^3, a threshold voltage V_{TH} of -16 V, and a subthreshold slope $S \equiv d(V_{gs})/d(\log_{10}I_d)$ of 2.7 V/decade. The hole field-effect mobilities μ_h of the *p* channel TFT extracted from the linear and saturated regimes are 0.023 and 0.031 cm^2/Vs, respectively. The ON/OFF current ratio of the *n channel TFT* of Figure 38 (b) is ~ 10^4, its V_{TH} is 3 V, and S = 4.2 V/decade. The electron field-effect mobilities μ_n of the *n* channel TFT extracted from the linear and saturated regimes are 0.72 and 1.0 cm^2/Vs, respectively. These μ_n values lie substantially below those obtained in a separately fabricated μc-Si *n* channel TFT. We ascribe the reduction in field-effect mobility to the unoptimized process sequence for CMOS inverter fabrication, which also is reflected in the values for V_{TH} and S.

The voltage transfer characteristic of the *CMOS inverter* made of the pull-up *p* channel TFT and the pull-down *n* channel TFT is shown in Figure 39 for supply voltages of V_{DD} = 30 V and V_{SS} = -20 V. The inverter exhibits a nearly full rail-to-rail swing, and an abrupt and well-defined voltage transfer characteristic with a gain of 7.2. The output HIGH is about 90% of the full voltage range and the output LOW is at the same voltage as V_{SS}.

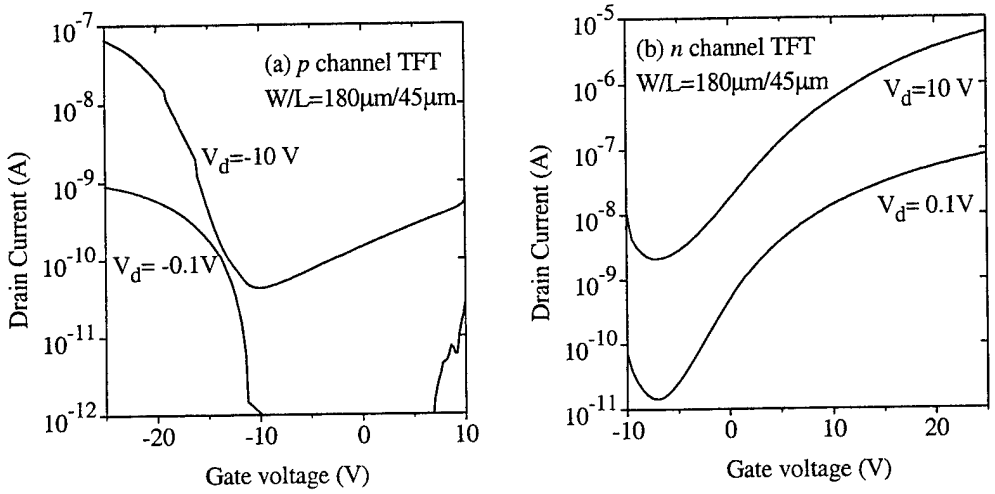


Figure 38 . Transfer characteristics of the (a) *p* channel nc-Si TFT, and (b) *n* channel nc-Si TFT of the CMOS inverter.

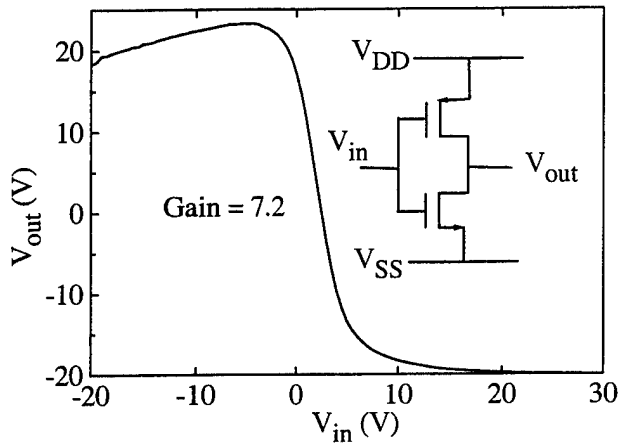


Figure 39. Voltage transfer characteristics of a CMOS inverter made of μc-Si. The *p* channel and *n* channel TFTs have identical channel dimensions. V_{DD} = 30 V and V_{SS} = -20

Thus, we have introduced a digital device and circuit technology based on directly deposited microcrystalline thin-film silicon. Its maximum process temperature of 320°C is ideally suited to glass substrates, and of course is suitable to more refractory substrates such as steel. It also is suited as a complementary metal-oxide-silicon (CMOS) technology for add-on circuits to application-specific integrated circuits (ASICs). The μc-Si TFTs need improvements in two directions. One is higher field effect mobilities, to enable higher ON current for high speed and high fan-outs. The other is a further reduction in process temperature, to take advantage of a wider variety of substrate materials. We are confident that progress can be made in both directions.

nc-Si TFTs made at 150°C

Our measure of material quality is the carrier mobility in saturation, μ_{sat}, which best reflects the capability of the channel material as the saturation current is not affected by charge trapping. We extract μ_{sat} from the saturation currents of the devices shown in Figures 40 (a) and (b), as $\mu_{sat} = 2\,(L/W)\,(t_{ox}/\varepsilon_{ox})\,[I_{DS}/(V_{GS}-V_{th})^2]$, where L and W denote the channel length and width, t_{ox} is the thickness of the dielectric layer and ε_{ox} is the dielectric permittivity. Because the threshold voltages vary because of charge trapping, we conservatively use a value of V_{th} = 0 V for all devices. The p-channel structures have mobilities $\mu_{sat,h}$ of ~ 0.06 $cm^2V^{-1}s^{-1}$ (150°C p^+) and ~ 0.2 $cm^2V^{-1}s^{-1}$ (280°C p^+), and in the n-channel structure the electron mobility $\mu_{sat,e}$ is ~ 12 $cm^2V^{-1}s^{-1}$. Because of insufficient electrical activity of the doped layers and excessive trapping and de-trapping in the gate dielectric, we consider these mobility values to be lower limits of actual channel capability. However, they prove that the nc-Si:H channel layer made at 150°C is adequate for CMOS operation. Because we deposit the nc-Si:H by the PECVD technique that already is employed for solar cells and liquid-crystal display backplanes, our results suggest that large-area CMOS from nc-Si:H deposited on low-temperature substrates (polymers) is feasible.

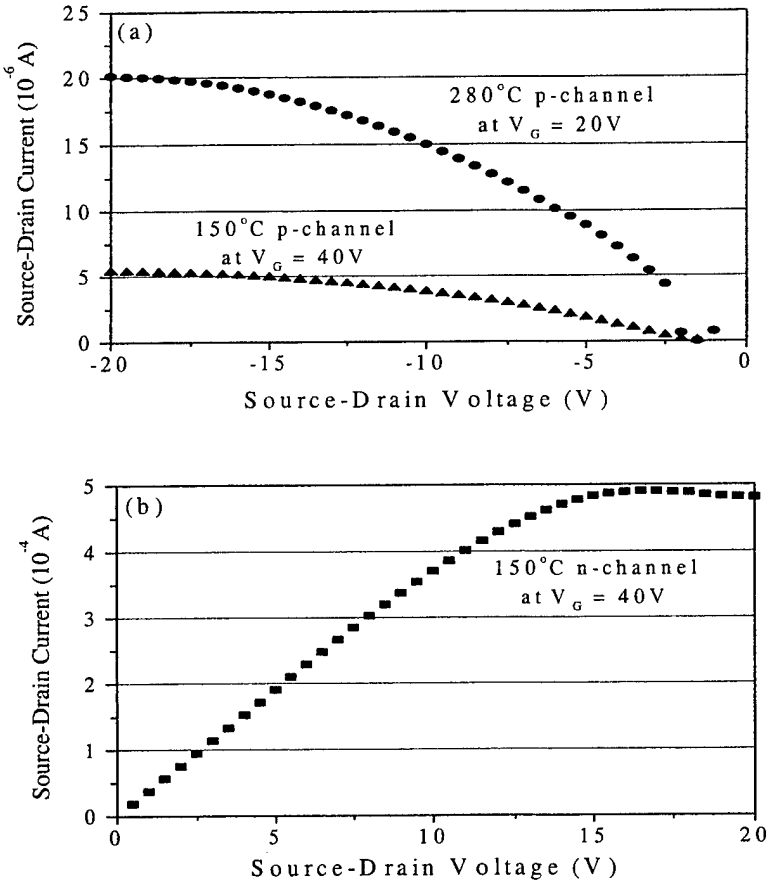


Figure 40 Field effect current-voltage characteristics of (a) two p-channel devices with p^+ layers fabricated at 280°C or at 150°C, and (b) an n-channel device fabricated at 150°C.

Effects of mechanical bending on the electrical performance of a-Si TFTs

Upon application of compressive strain we observed a slight decrease in the on-current I_{on}, and hence the linear mobility. The changes in the off-current I_{off}, leakage current I_{leak}, threshold voltage V_{th}, and subthreshold slope S remained within the experimental error and we concluded that they do not change. The mobility decreased linearly with increasing compressive strain, as shown in Figure 41, which depicts the mobility ratio μ/μ_0 as a function of compressive strain η, where μ is the linear mobility under set compressive strain and μ_0 is the initial linear mobility. Each symbol on the graph represents a different TFT. The identical empty and full symbols correspond to TFTs bent perpendicularly to the channel direction and measured with 'soft' and 'hard' probes, respectively. The half-shaded squares depict the change in mobility for TFTs measured with 'soft' probes while bent parallel to the channel. There is no qualitative difference in the behavior of μ/μ_0 as a function of strain, but quantitatively the parallel bending direction and 'hard' probes give slightly larger values of μ/μ_0. A linear fit to all experimentally measured mobilities gives: $\mu/\mu_0 = 1 - \eta/4$, when the strain is expressed in percent. For a given compressive strain, the drop in the mobility was 'instantaneous' (on the time scale of 5 minutes)

and it did not change further during the measurement time of ~ 40 hours. No change in the off-current or leakage current was observed.

In crystalline silicon the electron and hole mobilities depend on scattering mechanisms, the most important of which are scattering by thermal vibrations of the lattice and scattering by ionized impurities. During our bending experiments the amorphous silicon network is squeezed by no more than 1%, which causes an insignificant change in the scattering length. The measurements are performed at constant temperature. The a-Si:H is of device quality and does not contain phosphorus or boron impurities. However, in amorphous silicon TFTs the free electron mobility is reduced to an effective mobility by frequent trapping in the conduction band tail states. Thus, the electron field effect mobility depends on the width of the conduction band tail. For these reasons we considered a change in the slope (width) of the conduction band tail under compressive strain as the cause of mobility reduction.

Welber and Brodsky showed experimentally that the optical band gap E_g of a-Si:H decreases with increasing hydrostatic stress as $(\partial E_g/\partial P)_T \sim -1\text{x}10^{-11}$ eV/Pa, where P is the applied pressure (compressive stress). E_g decreases slowly in the low-pressure region, accelerates for pressure larger than ~ 2 GPa, and an irreversible change in E_g is observed for pressure larger than ~ 5 GPa. The compressive strain of 1% of our experiment falls into the low-pressure region. Using a value of 183 GPa for the Young's modulus of the TFT stack and 0.22 for the Poisson ratio we calculated that the optical gap of a-Si:H is reduced by ~ 23 meV under compressive strain of 1%.

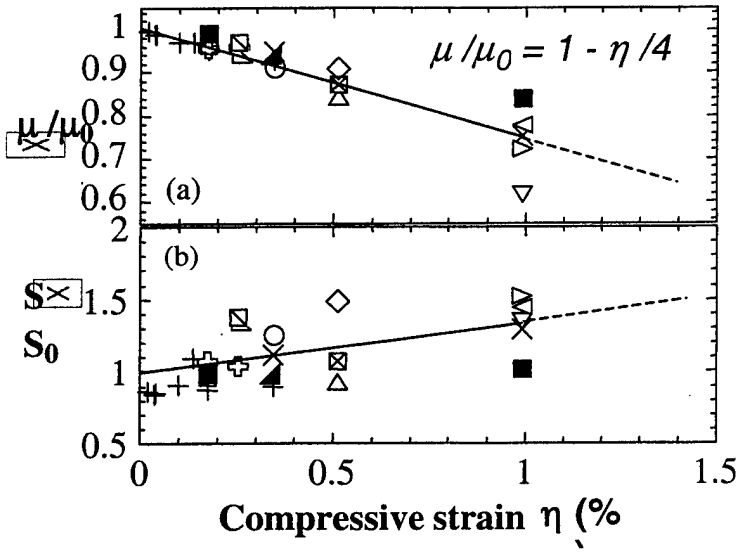


Figure 41. Relative mobility (a) and relative subthreshold slope (b) plotted as a function of compressive strain. Each symbol represents a different TFT. Empty and full symbols correspond to TFTs with the bending direction parallel and perpendicular to the source-drain current path, respectively.

Cody et al. found that in a-Si:H both the optical gap E_g and the Urbach energy E_0 are controlled by the amount of disorder, structural and thermal, and are correlated as $\Delta E_g \sim -6.2 \Delta E_0$. Following this formula, a 23-meV-reduction in E_g would cause an increase in E_0 of ~ 3.7 meV. It is plausible to assume that compressive stress will cause an increased structural disorder in a-Si:H and hence the increase in E_0 and decrease in E_g.

Sherman et al. found in a-Si:H a correlation between the slope of the valence band tail (Urbach energy) and the slope of the conduction band tail. In addition, the electron linear mobility of a-Si:H TFTs correlates with the Urbach energy of the a-Si:H channel material. The Urbach energy of our a-Si:H channel material is ~ 52 meV. Following the argument of the preceding paragraph, under the compressive strain of 1% this value is likely to increase to 55.7 meV. Using Sherman's correlation, the linear mobility of our a-Si:H TFTs then might decrease by as much as 50%. We observed an average decrease in the linear mobility under the strain of 1 % of only about 25%.

3.2 Electronic Materials Printing – Sturm (Princeton)

3.2.1 Ink Jet Printing: Introduction

Polymer OLEDs are a promising technology for flat panel displays [1]. These devices typically consist of a multi-layer sandwich of a transparent substrate, a transparent anode (in our work, Indium Tin Oxide), a thin film of an organic polymer blend (in our work, the hole-transporting polymer Poly(N-vinyl carbazole) (PVK) doped with an emissive dye), and a reflecting cathode. (The device structure and principle of operation are illustrated in Figure 42.) When current is driven through the device, holes from the anode and electrons from the cathode combine in the organic film to form excitons, which emit light as they decay. It has been shown that by doping the organic active layer with a small amount of dye one can tune the emission wavelength [2]. Currently, spin coating is the standard method for depositing a polymer blend film, which produces a uniform layer of polymer. However, this does not allow one to integrate multiple colors onto a single substrate, because the film is the same everywhere.

It has been proposed previously [3,4] to locally dope an initially undoped PVK film by depositing droplets of a dye solution onto the film surface and allowing the droplet to evaporate. This task is ideally suited to IJP. This basic procedure is outlined schematically in Figure 43. To integrate red, green, and blue devices onto a single substrate, solutions of red, green, and blue dyes are locally printed onto the same substrate. Our objectives in developing this technique are to (a) produce a uniform dye distribution over the device area and film depth and (b) maintain the initial film morphology (so that the electrical device characteristics are not degraded). In employing IJP, this technique should be relatively inexpensive to perform and applicable to large area substrates.

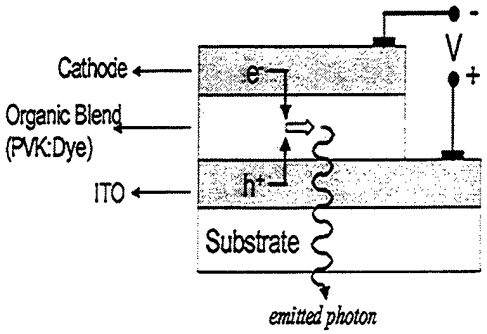


Figure 42. Basic OLED structure.

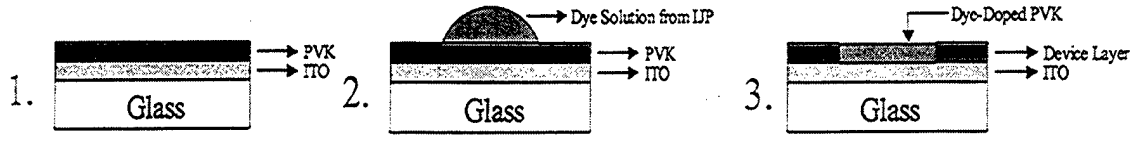


Figure 43. Procedure for dye-doping by ink jet printing. [3.4]

Ink Jet Printing: Approach

Our experimental apparatus consists of a piezo-electric type ink jet printer (supplied by MicroDrop GmbH) with a glass print head (which is therefore resistant to solvent damage) and x-y-z print head stage motion. In addition, our system has integrated digital imaging equipment, allowing us to view droplet ejection from the print head nozzle directly and to view drying droplets (from above) under high magnification. The print nozzle consists of a 25 μL capillary cavity surrounded by a piezo-electric sleeves which can contract and expand the fluid cavity (see Figure 44). To drive a droplet out of the nozzle, a first positive then negative pressure pulse is applied to the fluid through the voltages applied to the piezo-electric sleeve. The positive pulse drives the fluid down into the nozzle tip (which is 50 μm in diameter), and if sufficient energy is supplied by this pulse, a droplet (with diameter slightly larger than the nozzle diameter) will be ejected. The essential free parameters for controlling droplet ejection are the piezo voltage and the pulse duration.

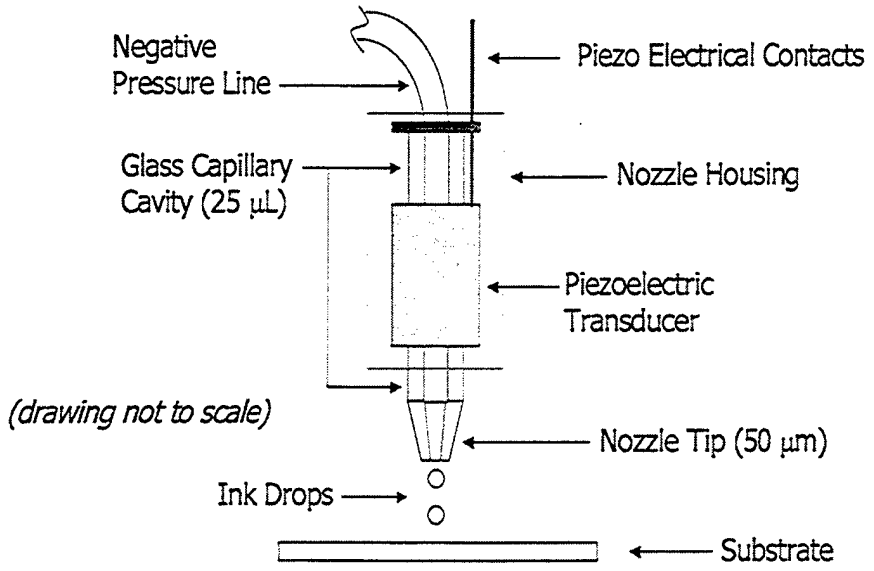


Figure 44. Schematic of Ink Jet Nozzle. (The negative pressure line is used to balance gravitational forces.)

Several parameters are relevant to understanding droplet formation from an ink jet printer: system geometry (i.e. of capillary cavity and nozzle), properties of the fluid being printed (i.e. viscosity, surface tension, and density), and the relationship between the applied voltage and the resulting pressure pulses. Even if each of these parameters is known in detail, a closed-form analysis of the governing Navier-Stokes equations is not possible. However, there is a rapidly growing literature on approximate solutions and numerical simulations of ink-jet flow (e.g. [5-7]), and some important trends are observed.

Ink Jet Printing: Results and Discussion

Droplet formation can be divided up into four regimes, based on the applied voltage. At very low voltages, no droplet is ejected, because the applied pressure pulse has insufficient energy. At higher voltages, single, stable droplet ejection is observed. At still higher voltages, satellite droplets are observed along with the main droplet, and this regime is generally less stable than the single droplet regime. Finally, at yet higher voltages, the ejected fluid will not form into a main droplet and satellites, but break up into an uncontrolled spray, or "jet." These four regimes were clearly demonstrated experimentally on our system with Dimethyl Sulfoxide (DMSO) (see Figure 45).

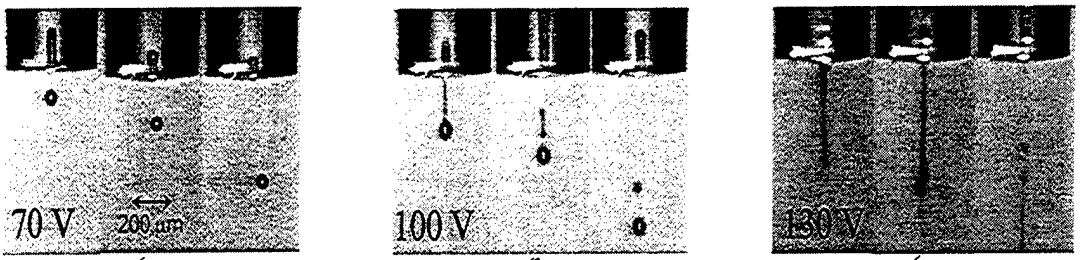


Figure 45. Observation of droplet formation regimes with DMSO. No drops were observed for voltages below 60V. (a) Single droplet regime. (b) Satellite droplet regime. (c) "Jet" regime.

We investigated droplet formation with numerous solvents, and found that we could not form droplets (stable or otherwise) at any voltage or pulse duration for solvents with low viscosity and low surface tension on our system. This phenomenon is not reported in the literature. Nevertheless, this introduced a new constraint on solvent selection for our work. The results of our solvent IJP characterization experiments are summarized in Figure 46.

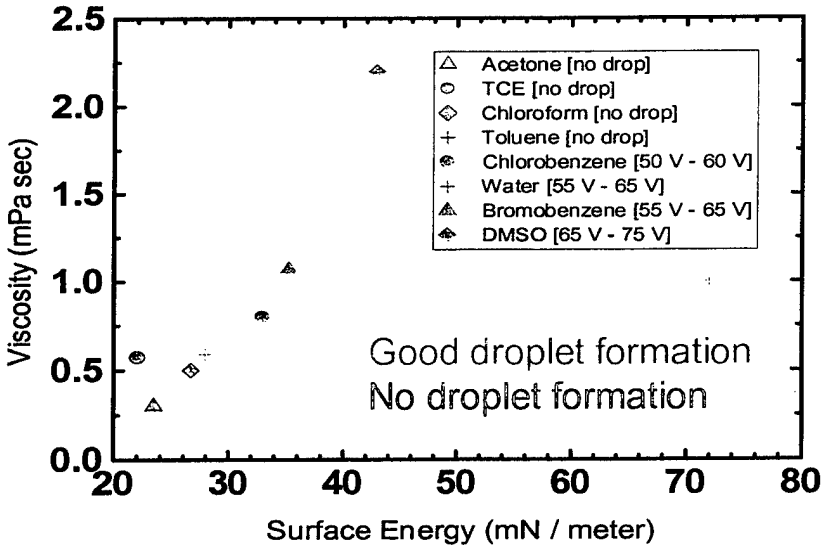


Figure 46. IJP Solvent Space. For printable solvents, the voltage range for the single droplet regime is given in the legend in brackets.

Once a droplet of dye solution is deposited on the polymer film, the actual dye doping occurs over the course of the evaporation of the solvent. Understanding how the dye is laterally distributed in the film, therefore, requires an understanding how a droplet dries. There are essentially two basic types of drying: unpinned and pinned (see Fig. 47).

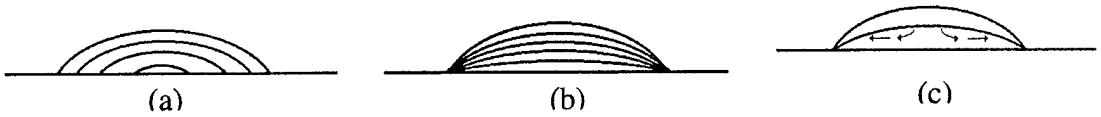


Figure 47. Evaporation phenomena. (a) Unpinned. (b) Pinned. (c) Flow during pinned evaporation.

It is well known that a droplet of fluid on surface has a characteristic contact angle, θ_c, which is dependent primarily on the fluid-surface interface (and only weakly on the surface-air and fluid-air interfaces). In unpinned evaporation, θ_c remains constant as fluid from the droplet surface evaporates, and the droplet radius shrinks correspondingly. In pinned evaporation, the droplet radius remains constant, and instead θ_c shrinks. Though the phenomenon of pinning is not fundamentally understood, it has been proposed that it is the result of surface roughness (including possible "self-roughening" by solute deposition) [8-10]. In addition, it is believed that for the droplet radius to remain constant during evaporation, fluid must flow out from the center to the edge of the drop, leading to a possible mass flow of solute towards the edges [8], as illustrated schematically in Figure 47.

Our first dye doping experiments were performed on ~100 nm PVK films, using a solution of the green emitting dye Coumarin 6 (C6) in acetone. Since we could not print acetone with our ink-jet printer, in these experiments we used a syringe to deposit individual droplets of ~11μL, which had a deposited radius of ~7mm. We found that for room temperature evaporation, the acetone droplet remained pinned at its initial radius for ~35 s, and then its radius fell rapidly during the remaining 15 s of evaporation (see Figure 48a). The resulting dye distribution was observed under ultraviolet (UV) photoluminescence (PL) (see Figure 48b), and revealed distinct rings of high dye concentration corresponding to droplet pinning, while between the rings, the dye concentration was very low. This observation of dye pile-up into rings was further confirmed by X-ray microprobe. These results clearly demonstrated that mass transport of solute from the center of the droplet to the edges (through some mechanism) occurred. Reducing the evaporation rate by cooling the substrate to 4°C greatly improved the dye distribution uniformity over the droplet area; however, substantial segregation of dye towards the edges was still clearly observed.

Many solvents were considered when determining the best choice for our initial IJP experiments. Essentially, we required a *printable* solvent that dissolved the dye and not the PVK films we would be printing on. In addition, because our work with acetone suggested that slower evaporation times would improve the dye distribution, we desired a solvent with a low vapor pressure. Among the common solvents we tried, DMSO was the only one to meet all these requirements (see Table 3).

Table 3. Solvents Investigated for IJP Dye Doping Candidacy. (All values for 25°C.)

Name	Formula	Viscosity* (η) (mPa·s)	Surface Energy* (γ) (mN/m)	Vapor Pressure* (p_v) (kPa)	Dissolves Dyes	Dissolves PVK	Prints
Chlorobenzene	C_6H_5Cl	0.753	32.99	1.6	Yes	Yes	Yes
Cyclohexanone	$C_6H_{10}O$	2.02	34.57	0.53	Yes	Yes	Yes
Tetrachloroethane	$C_2H_2C_{l4}$	1.84	35.58	1.6	Yes	Yes	Yes
Dimethyl sulfoxide	**C_2H_6SO**	**2.20**	**42.92**	**0.08**	**Yes**	**No**	**Yes**
Water	H_2O	1.00	71.99	1.00	No	No	Yes
Chloroform	$CHCl_3$	0.58	26.67	26	Yes	Yes	N
Acetone	C_3H_6O	0.30	23.46	31	Yes	No	No

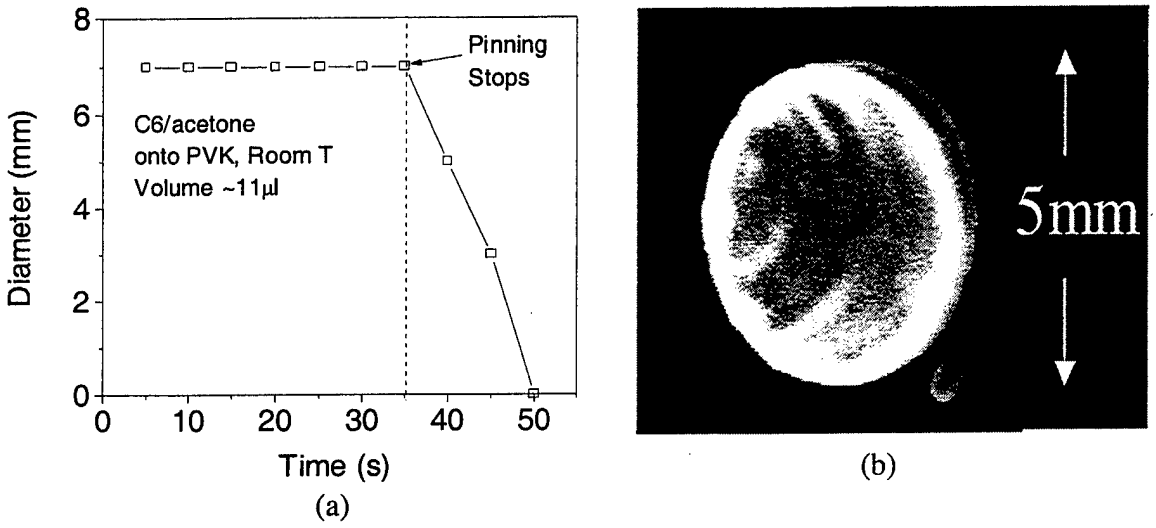
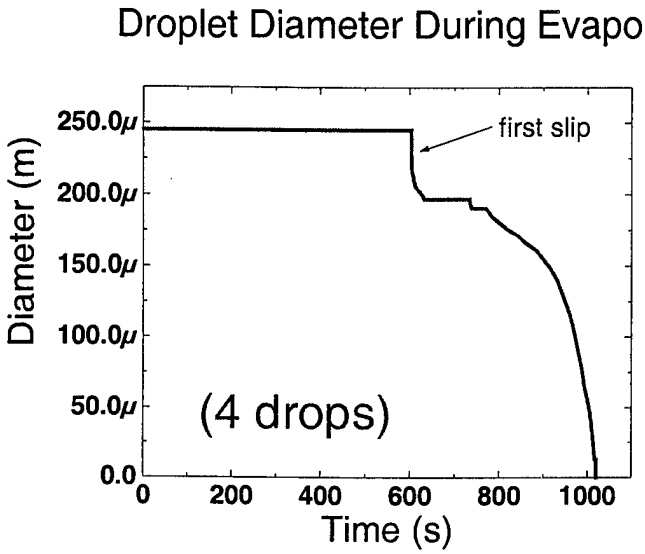


Figure 48. Acetone:C6 Deposition.
(a) Droplet radius with time during evaporation.
(b) Photoluminescence of dye doping, where brightness corresponds to C6 concentration.

We printed droplets of C6 in DMSO onto PVK films, and observed the drying phenomena. We found that the droplet was pinned for the first 600 s, and for the remaining 400 s evaporation proceeded through a complex sequence of pinning and slipping (see Figure 49a). The resulting dye distribution was observed using a PL image of the droplet, which revealed a fairly uniform dye distribution, but with a noticeable segregation of dye towards the center (see Figure 49b). There were no high concentration outer rings observed as in the acetone results. Closer inspection of the PL image shows that instead, a small number of thick, circular bands of uniform dye distribution are present around an essentially uniform central region, with increasing dye concentration towards the center. The edges of these regions correspond well to the pinned radii observed during evaporation, suggesting that in a region of PVK suddenly exposed by a droplet slip, the absorbed solvent evaporates without any dye redistribution. This is consistent with the assumption that the evaporation of the solvent absorbed into the ~100 nm film should occur extremely rapidly and evenly over the exposed film area. (This result also suggests that in the PVK *under* the solvent droplet, the dye concentration is uniform at the time of the slip.)

(a)



(b)

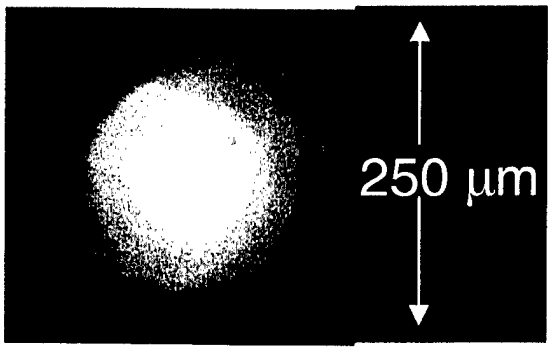


Figure 49. DMSO:C6 IJP Deposition.
(a) Droplet radius with time during evaporation. (b) Photoluminescence of dye doping.

We fabricated integrated red, green, and blue electrical devices on a single substrate, using the dyes Nile Red, C6, and Coumarin 47 to produce each respective color. The resulting 250 μm devices demonstrated similar electrical characteristics to spin-coated devices without IJP, suggesting that the IJP dye doping process did not adversely affect the electrical behavior of the PVK film. The observed electroluminescence (EL) was investigated for uniformity, and an image of 3-color integrated devices is in Figure 50.

The color uniformity is good over most of the device area, however, there is a distinct dark spot observed in the center of the device, with a slight darkening of the luminance just around this spot. The increased dye concentration in the center of the device (observed in the PL results) could explain a darkening of the luminance (due to dye concentration quenching [11]) in the center, but this effect cannot explain the sharp, completely dark spot observed. This dark spots appears to be correlated with the surface deposition of some material during the extremely fast drying which occurs in the last stages of the evaporation process over a total region with a radius of about 20 microns, but the details are still unknown.

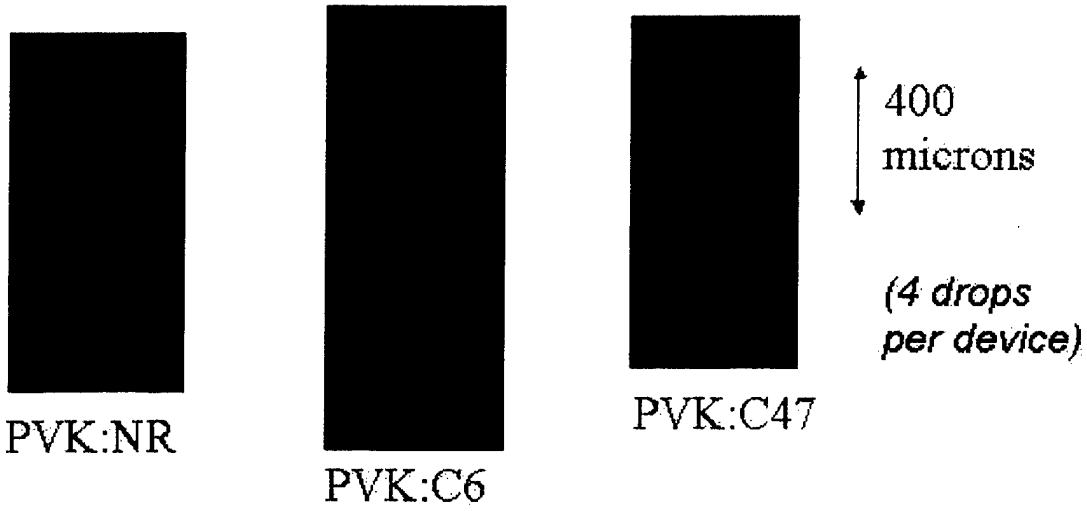


Figure. 50. Electroluminescence of integrated 3-color IJP dye doped OLED's. The origin of the central dark spot is under investigation

Ink Jet Printing: Conclusions and Recommendations

We have developed a system to investigate the dye doping by IJP of polymer OLED's, including a highly controllable all-glass ink jet printer and digital imaging equipment for studying IJP droplet formation and droplet drying phenomena. Using a very low vapor pressure solvent, uniform dye distribution over the droplet area was achieved. The dye distribution is critically affected by the dynamics of the drying process, which at present are only qualitatively understood. Integrated 250-micron RGB devices were demonstrated with good color uniformity and with electrical properties comparable to spin-coated devices without IJP.

This work shows that ink-jet printing can fundamentally be used for OLED manufacturing. However, the results depend critically on the organic material system and the exact details of the printer, due to requirements for stable droplet formation and due to the drying dynamics of the solvent/organic mixture. The critical issue is to assure a uniform profile across the pixel. There are two recommendations. First, the droplet drying process is not fundamentally understood, so further science in this area is required, especially in complicated prepatterned structures as would be used in real devices. Second, to realistically address the problems of drying profile and droplet formation for a production environment, joint work between the display system manufacturer, organic materials supplier (OLED materials expert), and the printing tool company will be required.

3.2.2 Dry patterned dye transfer: Introduction

Several methods have been suggested to laterally pattern the polymer layer to achieve RGB pixels. Among these methods are conventional photolithography on top of the polymer layer [1-4], photobleaching of dye [5], plasma etching of the organic film and subsequent spin-coating of another polymer layer [6], ink-jet printing of the polymer solution onto the substrate [7, 8] or printing a solution containing the dye onto a substrate which was previously deposited polymer film [9, 10].

We have previously demonstrated that a large-area dye diffusion can locally change the emission color [11, 12]. In this case, the emissive dye is diffused into the spin-cast polymer layer from a large-area dye source. This dye source consists of a flat substrate coated with a layer containing the dye to be diffused. To pattern the polymer layer of the OLED, a shadow mask was placed in between the dye source and the device substrate during the diffusion process at elevated temperatures. Typical conditions to transfer the dye and initially change the emission from blue to green or red are 40 min at 70 °C. However, due to the roughness of the steel shadow mask used in early experiments (which was placed in intimate contact with the device substrate), the polymer film was often damaged resulting in short circuited devices. This report will focus on two issues. First, it will describe recent progress to eliminate this shortcoming using either soft masks or a flat patterned dye source. Second, after the initial dye transfer at 70 °C, the dye profile is not uniform and it is hard to repeat results. Therefore a solvent-assisted method is introduced to temporarily reduce the glass transition temperature by 100 C, so that the dye can rapidly diffuse at room temperature.

Dry patterned dye transfer: Approach

The proposed processing of the OLED substrate is shown in Figure 51. After spinning a uniform polymer onto the substrate (usually patterned ITO for an active or passive matrix), dye molecules are locally introduced into the polymer. They change the emitting color of the OLED made in the polymer. The dye molecules are transferred from a dye source plate. The pattern is achieved by using an intermediate physical mask as shown in Figure 51, or by patterning the dye source layer itself as shown later.

The OLED polymer film was deposited on a glass substrate coated with indium-tin-oxide (ITO) (30Ω/cm^2). The polymer used was poly(9-vinylcarbazole) (PVK, MW~ 1 100 000 g/mole, 71.5% by weight in the final solution) as the hole transport material and 2-(4-biphenylyl)-5-(4-*tert*-butyl-phenyl)-1,3,4-oxadiazole (PBD, 28.5% by weight in the final solution) as the electron transport material [13]. Both, the PVK and the PBD, were obtained from Aldrich and used as received. The polymer blend also contained the dye 9,10-dioxa-*syn*-dimethylbimane (bimane, emission peak at 435 nm) [14]. The dyes diffused into the polymer film are coumarin 6 (C6, emission peak at 505 nm, obtained from Lambda Physik), and Nile red (emission peak at 580, obtained from Aldrich). Because the polymer blend already contains the blue dye, only two diffusion steps for the red and the green dye are required.

Results illustrating the basic concept are shown in Figure 52. Note that the electroluminescence emission peak changes from near 450 nm (blue) to ~500 nm (green) as C6 dye is added to a film which initially contains only a blue dye. (A key refinement of this approach described below is the use of solvent vapor to increase the vertical diffusion of the dye through the polymer after its initial transfer.)

It should be noted that the electroluminescence (EL) emission of devices containing two or more dyes, such as that in Figure. 52.) is almost entirely governed by the dye with the longest wavelength [15,16,27]. PL is seen from both dyes, in contrast. The EL from one dye is fortuitous, since it allows RGB pixels to be achieved by using just two diffusion steps. One starts with a blue-emitting polymer or one with a larger bandgap doped with blue dye. This is then doped locally by green and red dyes in two patterning/diffusion steps. The areas with red and green dye emit only red and green, and the blue dyes in these areas do not emit [27]. Figure 53 shows the PL and EL spectra for a device bimane (blue dye) and C6 (green dye) for the dye concentrations of 0.3 mg bimane and 0.3 mg C6 in 100 mg PVK and 40 mg PBD. Note EL is only seen from the low bandgap (green) dye.

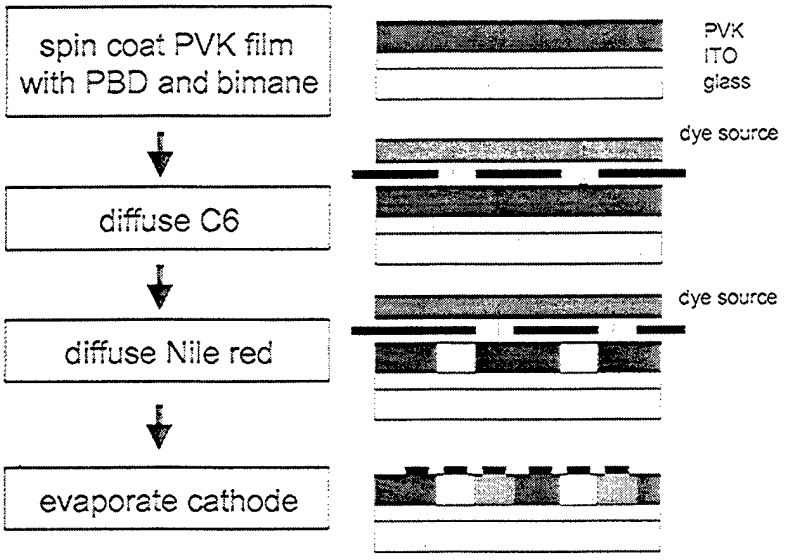


Figure 51. Schematic of dye diffusion process for a 3-color polymer OLED illustrating diffusion through patterned mask.[11,23].

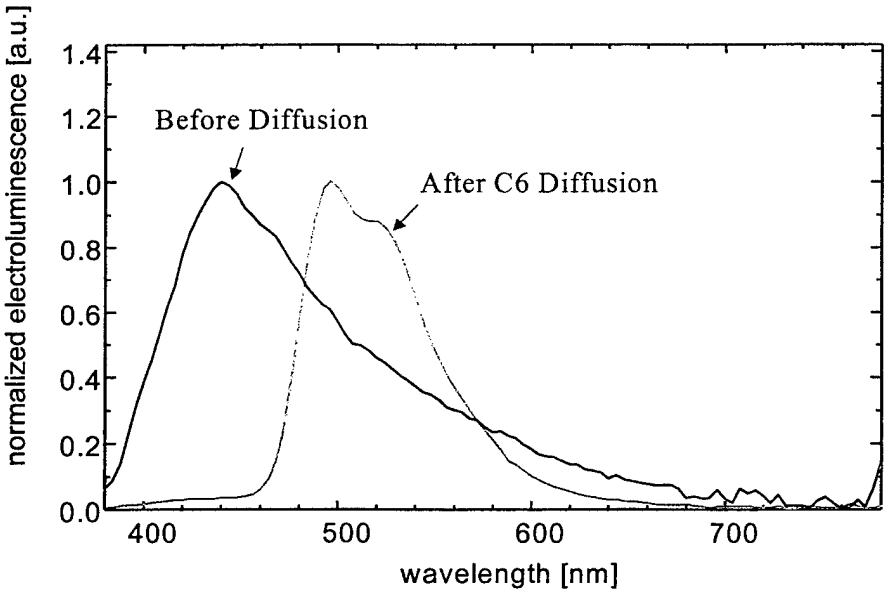


Figure 52. Photoluminescence of PVK OLED's (with 0.3 mg bimane (blue dye) in 100 mg PVK) before and after diffusion at 70 C of C6 from a dye source of 5% C6 in a PVK matrix.

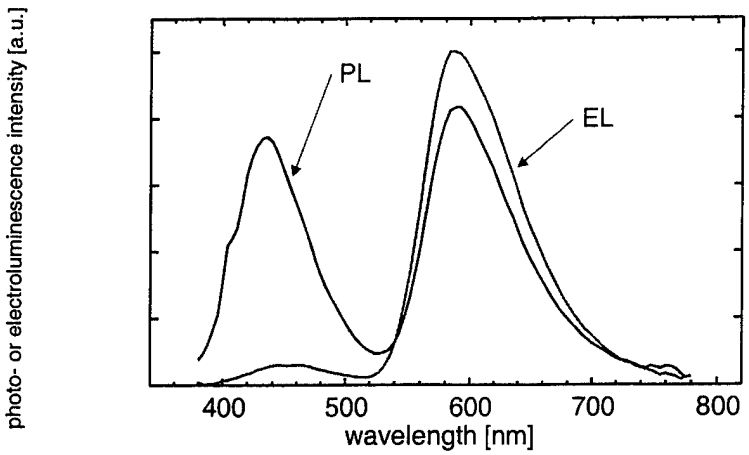


Figure 53. Photoluminescence and electroluminescence spectra of PVK/PBD devices with polymer spun on from solution with 0.3 mg bimane (emission peak at ~430 nm), 0.3 mg C6 (peak ~ 600 nm), 100 mg PVK and 40 mg PBD electron transfer agent [23]. Note difference in EL and PL spectra.

Dry patterned dye transfer: Results and Discussion

Soft Mask Development

To avoid the described problems of damaging the polymer film of the OLED during the dye diffusion process, the use of soft masks of organic materials is desirable. However, because of the sensitivity of the dye containing film of the dye source to solvents and spin-on photoresist, direct patterning of the dye-source was not feasible. We therefore laminated a pre-patterned polymer layer onto the dye-source substrate to prevent any disturbance of the dye-source film. The pre-pattered polymer layer was formed using a commercially available photoresist (obtained from DuPont, trade name Riston CM 206). It consists of a 16 μm thick photosensitive layer, which is sandwiched in between two supporting transparent plastic foils. After conventional photolithographic exposure, one of these foils was removed, and the photoresist, still supported by one transparent foil, was developed, followed by drying at room temperature. This film was then laminated at 150 °C using a simple commercial laminator onto the dye-source, which consisted of a glass substrate and a previously spun-on dye-containing film. This process is illustrated in Figure 54. The diffusion source for green and red emission was spin-cast from a solution containing 12 mg PVK and 50mg C6, or 13 mg PVK and 7mg Nile red, respectively. The masked dye source was then placed onto the polymer film of the device substrate. The diffusion process was carried out in vacuum at 70 °C for 40 min, with a pressure of 1500 Pa exerted on the dye-substrate. After the diffusion, the dye source/mask substrate was then separated from the OLED plate. For cathodes, the device substrate was coated with a Mg:Ag (10:1) cathode by thermal evaporation.

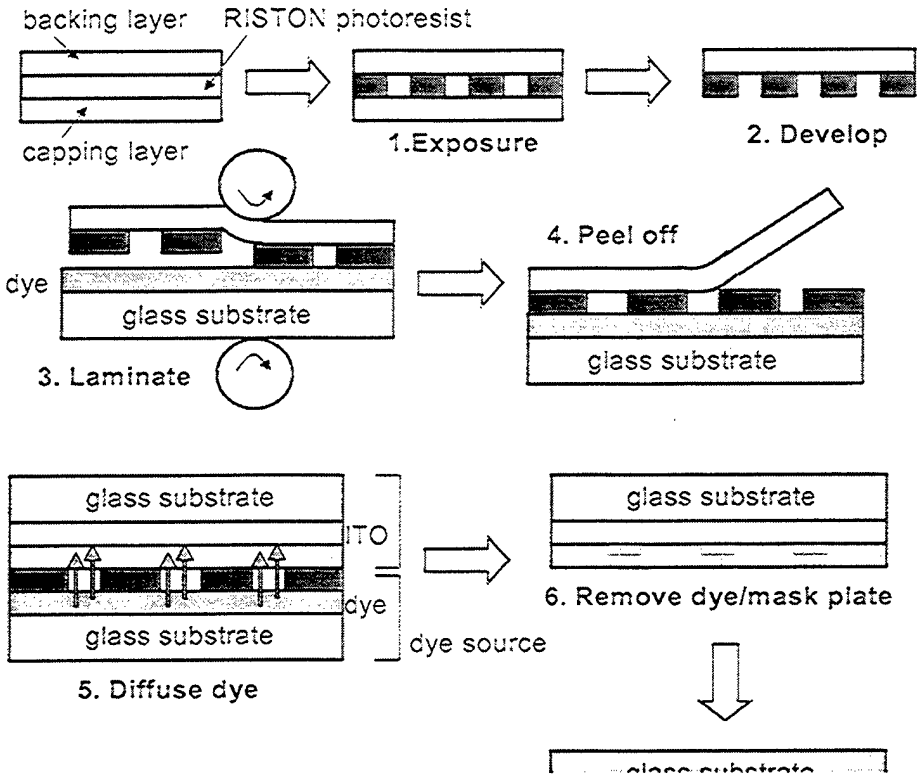


Figure 54. Use of transferred photoresist using a lamination process as mask for dye diffusion. The soft mask avoids the physical contact damage of a hard mask (e.g. stainless steel).

The IV-characteristic, along with the measured photocurrent due to light emission, of a diffused device on a un-patterned substrate is shown in Figure 55. In this experiment, we diffused C6 into a PVK/PBD layer (100 mg PVK, 40 mg PBD) using the same dye source as described above. The diffusion was carried out at 74 °C for 10 min. After the diffusion, the sample was annealed at 74 °C for 1 hour in vacuum. For comparison, two other devices were fabricated at the same time. Both of these samples were spun-on using a polymer solution, which already contained C6 (100 mg PVK, 40 mg PBD and 0.3 mg C6). One sample was coated with the metal cathode directly after the polymer deposition. The other sample was kept at 70°C for 1 hour in vacuum before the deposition of the cathode. The annealed device shows no significant change in their IV or photocurrent. So we conclude that the heat treatment at 70 °C has little intrinsic effect on the materials system. The diffused device has a similar IV curve to the other devices, but a much lower photocurrent. The decreased photocurrent is due to the lack of control of the amount of dye diffused into the polymer film. This is addressed later in the report with the solvent-enhanced diffusion method.

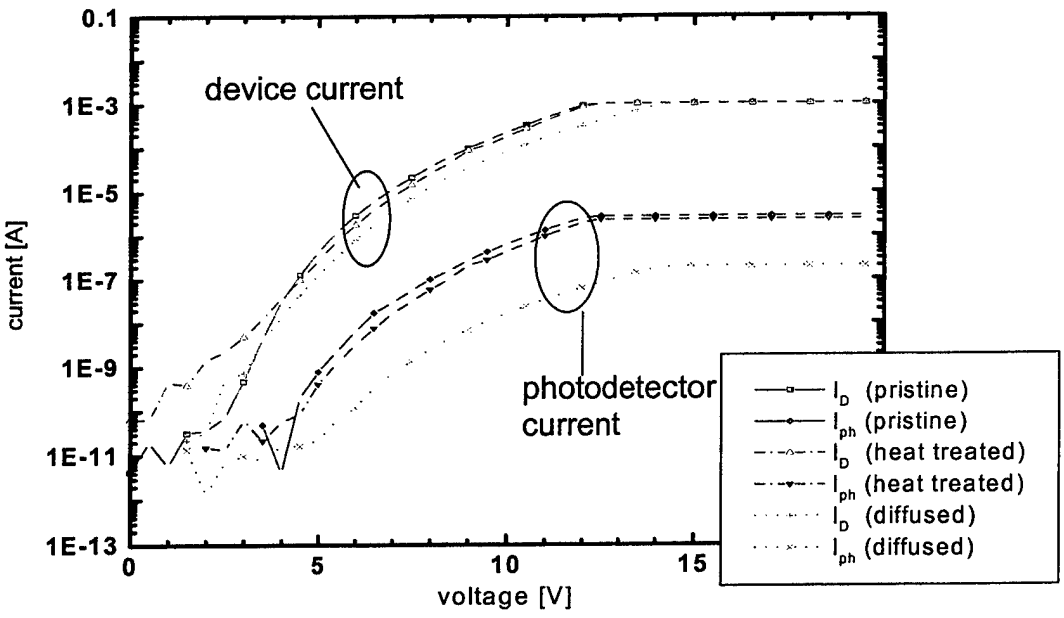


Figure 55. IV-characteristics and photocurrents of different devices with emitting area of 2 mm^2: (a) a device (PVK/PBD/C6) which was not exposed to heat at all, (b) a device (PVK/PBD/C6) which was kept at 70 °C for 1 hour under vacuum, and (c) a device (PVK/PBD only) with diffused C6 and subsequent anneal for 1 hour at 74 °C in vacuum.

In samples with a diffused pattern, lines of 20 μm width with a 40 μm pitch were observed by UV-excited fluorescence microscopy. The width was limited mainly by the resolution of the thick-film photoresist used (Figure 56(a)). An EL micrograph of a different pattern fabricated with the same technology is shown in Figure 56(b). No mechanical damage to the device was observed after the diffusion process. However, due to the contact of the photoresist with the polymer layer, a slight overall photoluminescence quenching was observed which occurred both in regions where the photoresist had been in contact with the device polymer film as well as in areas between the contact regions. Since the quenching may be due to out-diffusion of an undesired species in the photoresist, a process described in the next section was developed to avoid the presence of the resist during the diffusion cycle.

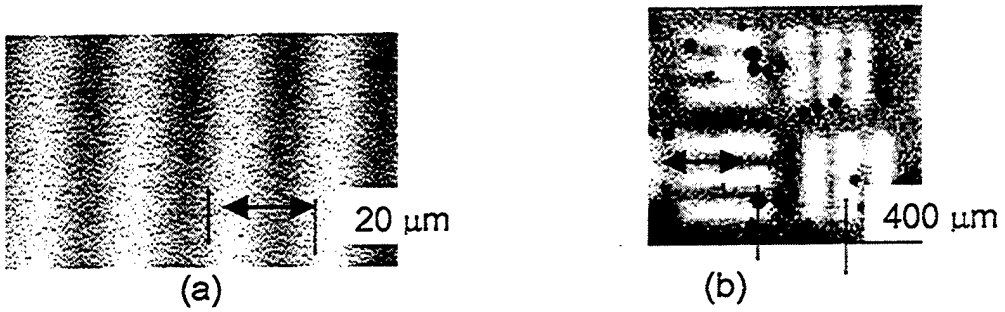
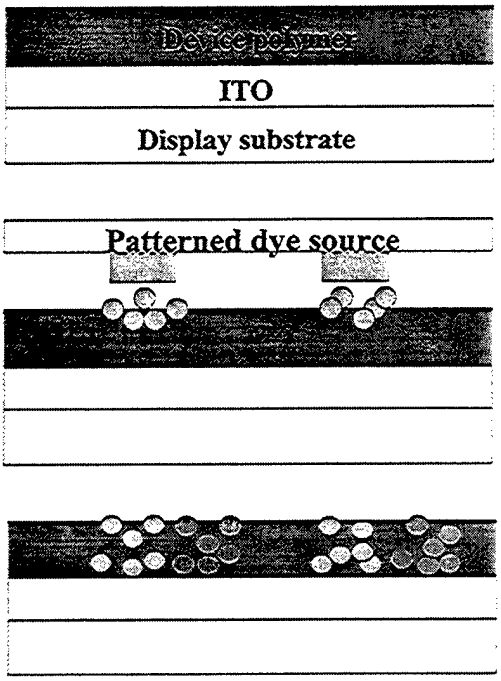


Figure 56. (a) PL micrograph and (b) EL micrograph of lines with C6 diffused into a film of PVK/PBD using a transferred photoresist mask

Dye Diffusion Using Patterned Dye Source:

To avoid any contact of the device polymer layer with any material other than the dye, we then used the laminated photoresist as an etching mask for the dye source. After the lamination of the photoresist onto the dye source (following the same steps described earlier), the substrate was then treated with an oxygen plasma. This process removed all organic material, which was not covered with photoresist. To remove the photoresist after patterning the dye-source film, a cleaned aluminum foil was laminated onto the dye source plate, making contact with the thick photoresist. Because of the good adherence of the aluminum foil to the photoresist layer, the photoresist could be simply lifted off, leaving only islands of the dye-source film on a flat glass substrate. The patterned dye-source substrate was then put into close contact with the device substrate with a pressure of 1500 Pa as shown in Figure 57. The dye diffusion was carried out at 70 °C for 90 min in air. The dye source was a spin-coated layer of the dye (few % concentration) in a host vylon polymer. Vylon was used because of its anti-stick properties to avoid damaging the device polymer when the dye source is physically separated from the device polymer after the printing step (transfer of the dye).



Step 1: Uniform spin-coat of device polymer with blue-emitting dye

Step 2: Dye Contact Printing: transfer of green dye from pre-patterned dye source to device polymer surface(~70 °C)

Step 3: Repeat printing with patterned red dye

Step 4: Diffusion of dyes vertically throughout the polymer film

Figure 57. Dye diffusion process using patterned dye substrate.

Figure 58 shows a micrograph of the electro-luminescence of a 3 mm high letter with 200 μm color features using the process of Figure58 (when an undoped device polymer was used and only nile Red was used in a single printing step, however). The outline of the letter is defined by ITO, and a blanket Mg:Ag cathode was deposited. The 200 μm bright stripes are lines where the dye Nile red was diffused into the PVK/PBD film. The polymer film itself emits only very weakly in the deep blue where no dye was added.

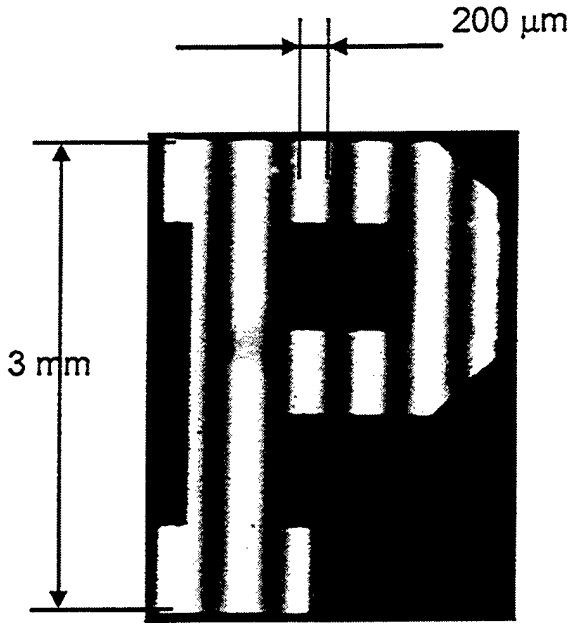


Figure 58. EL micrograph of a 3 mm high letter with 200 µm lines of diffused Nile red.

Thermal stability of the dye pattern

Both for modelling the dye diffusion process and for the long-term stability of the device, it is of major importance to know the diffusion rate of the dye in the PVK/PBD film. It is expected that the rates are very high above the glass transition temperature T_g and very small below it [17, 18]. For the PVK/PBD blend used in this experiment, T_g is approximately 125 °C [19]. To investigate the stability, we diffused C6 with a pattern of 20 µm and 40 µm pitch into a PVK/PBD film at 70 °C. The films were annealed and the change in PL vs. distance along the surface was used as evidence of lateral dye diffusion in the polymer. Initially, we observed anomalously high diffusion rates, which were found to be due to evaporation of dye, followed by gas phase transport and re-deposition onto undoped areas some distance away. To eliminate this effect, a 60 nm thick layer of $SiNO_x$ at 50 °C by Plasma Enhanced Chemical Vapor Deposition (PECVD) was deposited on the polymer surface. This solved the anomalous diffusion problem, and also helped to reduce any polymer degradation due to contact with air and water vapor at the annealing temperature. The photoluminescence image was taken using a fluorescence microscope. The samples were then annealed for four hours at 90 °C, 105 °C, 120 °C, or 135 °C. After anneal, a PL image was taken at the same spot, and compared to the one taken before the anneal (Figure59). We were unable to detect any lateral diffusion of the dye at annealing temperatures below 120 °C, but samples annealed at higher temperatures showed a slight lateral diffusion. By modelling the evolution of these profiles, the diffusion coefficient of dye was extracted and found to be $D = 7 \cdot 10^{-13} \pm 2 \cdot 10^{-13}$ cm^2/s for 120 °C and $D = 8 \cdot 10^{-12} \pm 4 \cdot 10^{-12}$ cm^2/s for 135 °C. No change could be detected within experimental resolution at temperatures of 90 °C and 105 °C.

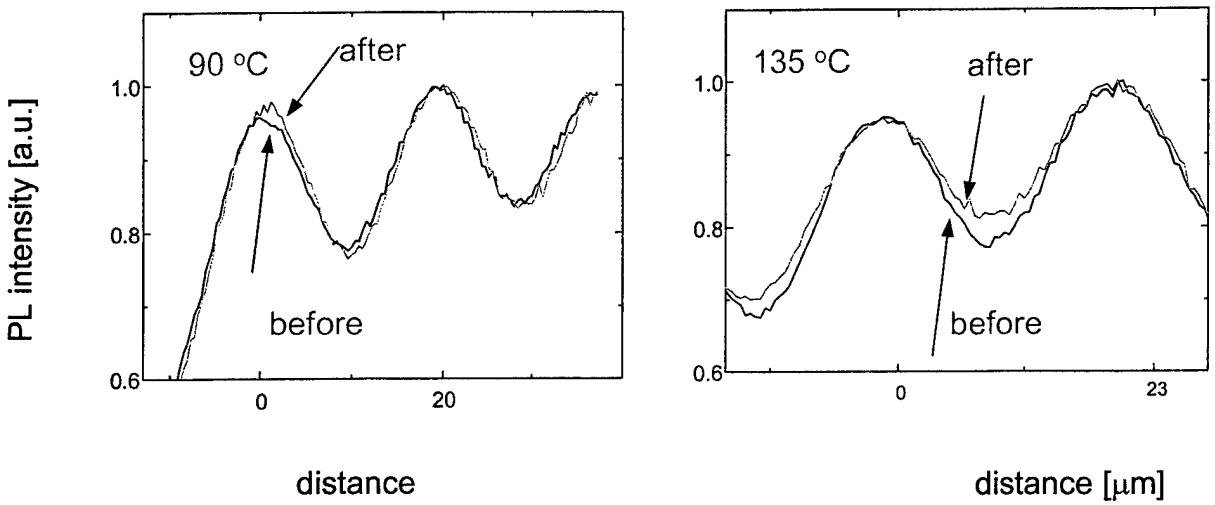


Figure 59. Spatial PL intensity profiles before and after 4 hour anneal at 90 °C or 135 °C of substrates with C6 stripes patterns diffused into PVK/PBD film.

Solvent Assisted Diffusion:

The initial dye transfer step (e.g. 70 °C) leaves most of the dye on the near surface of the target polymer film. Devices could be made at this point, but the highly peaked dye profile made the reproducibility of the devices hard to achieve. After the initial transfer step, to achieve a uniform distribution of the dye into the target PVK film, a diffusion temperature well in excess of 90 °C was required. Figure 61 shows the C6 profile after the an initial transfer step (as in Figure 57).This often led to degradation of the polymer. Thus a solvent-assisted diffusion method was invented, which reduced the diffusion temperature by over 100 °C.

Polymers are known to adsorb solvent from a vapor, leading to a volume expansion or "swelling effect". Qualitatively, this increased separation between polymer molecules increases the space through which dye molecules can diffuse. Alternatively, one may view the swelling as a reduction in the glass transition temperature. This process is shown schematically in Figure 60.

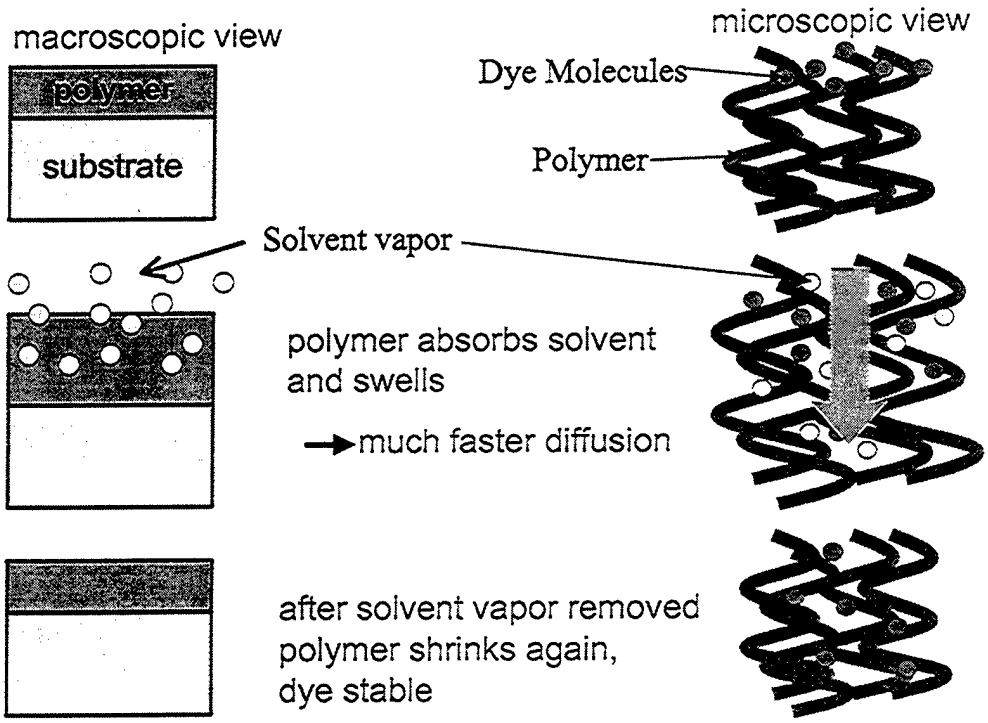


Figure 60. Schematic macroscopic and microscopic view of solvent-assisted dye diffusion. [24]

Figure 61 shows the profile of C6 dye after the initial transfer step at 70 C which leaves it mostly on the polymer surface. Annealing at 90 C or more in vacuum or nitrogen does little to further move the dye. However, if a small partial pressure of acetone is introduced, the polymer swells (volume expansion measured at ~15%), and the dye rapidly diffuses in a matter of minutes. For example, a typical ambient used is 0.5 ml of acetone in 1 liter of nitrogen, introduced into the diffusion chamber via a bubbling apparatus. The solvent vapor is then removed and the solvent outgases rapidly from the polymer. Figure 62 shows that the diffusion coefficient of the dye can be increased many orders of magnitude by this method at room temperature. At room temperature, a diffusion coefficient of 10^{-12} cm^2/s is observed with the acetone vapor, whereas without the vapor the diffusion coefficient is only 10^{-17} cm^2/s is observed at 90 °C, and by extrapolation (since we can't measure very low diffusion coefficients in a practical way), the room temperature diffusion coefficient would be only ~10^{-30} cm^2/s.

Using the approaches of patterned dye source transfer (red and green) followed by solvent-assisted dye diffusion, sharp lines of RGB-emitting polymers have been achieved over an area of 3 cm x 3.5 cm (Figure 63). RGB EL spectra using such a process are shown in Figure 64.

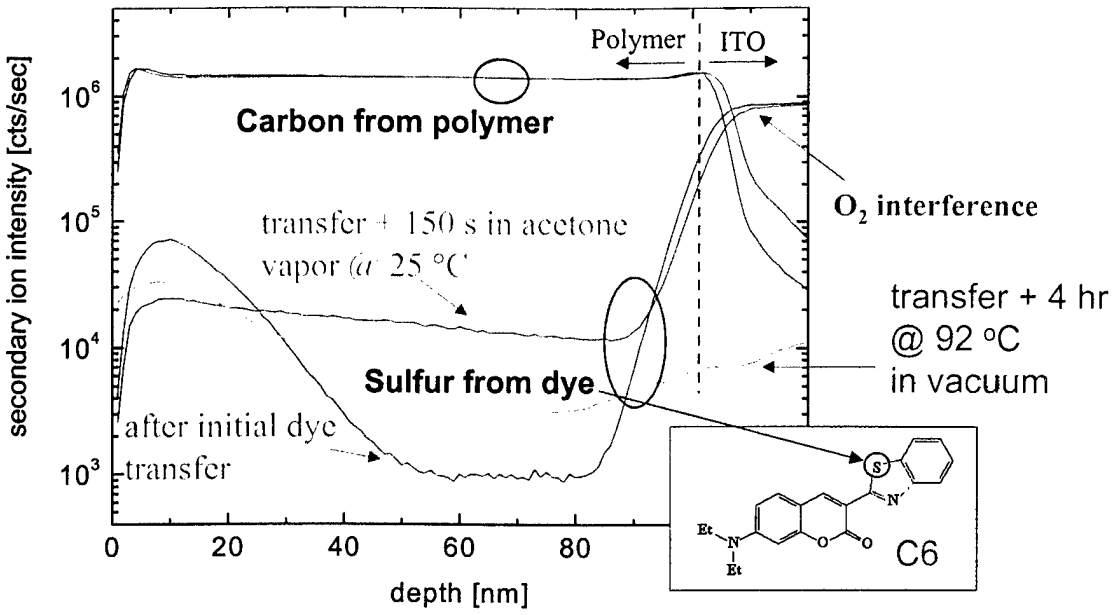


Figure 61. Depth profile by secondary ion masss spectroscopy (SIMS) of C6 dye into a PVK film after the intial dye transfer at 70 °C, followed by annealing at 92 °C for 4 hours, and after 150 sec annealing at 25 °C with no high temperature anneal after the initial dye transfer step. The ambient was 0.5 mg acetone per liter nitrogen. [24].

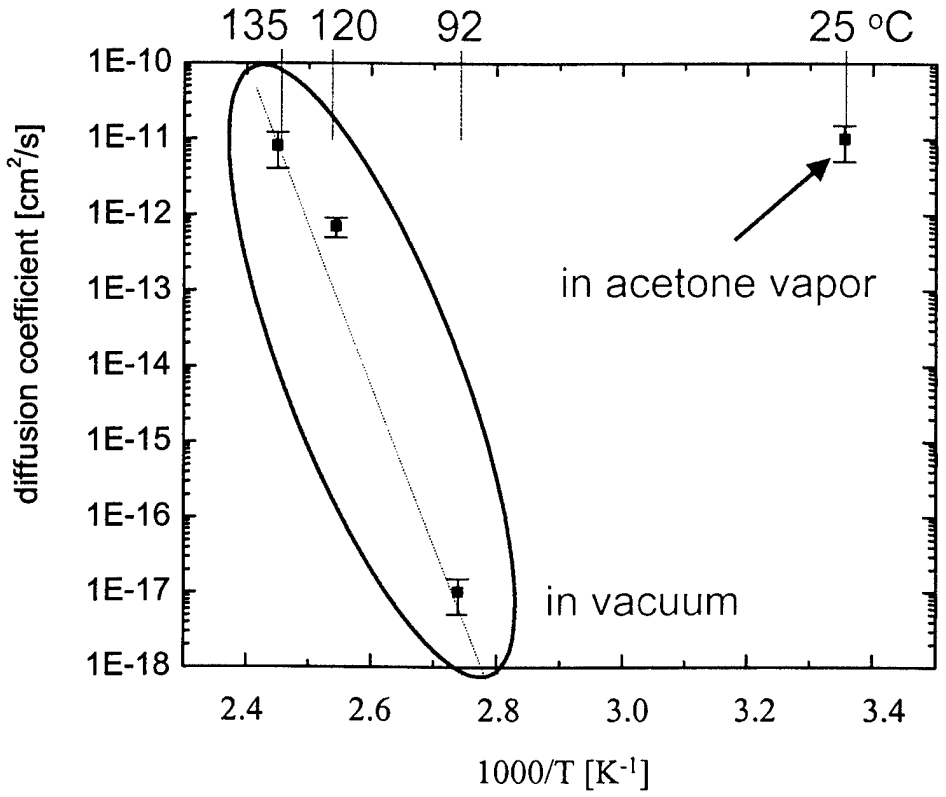


Figure 62. Diffusion coefficient of C6 dye in PVK as a function of inverse temperature in vacuum and in nitrogen with aceton partial pressue (0.5 mg per liter nitrogen) [24, 26].

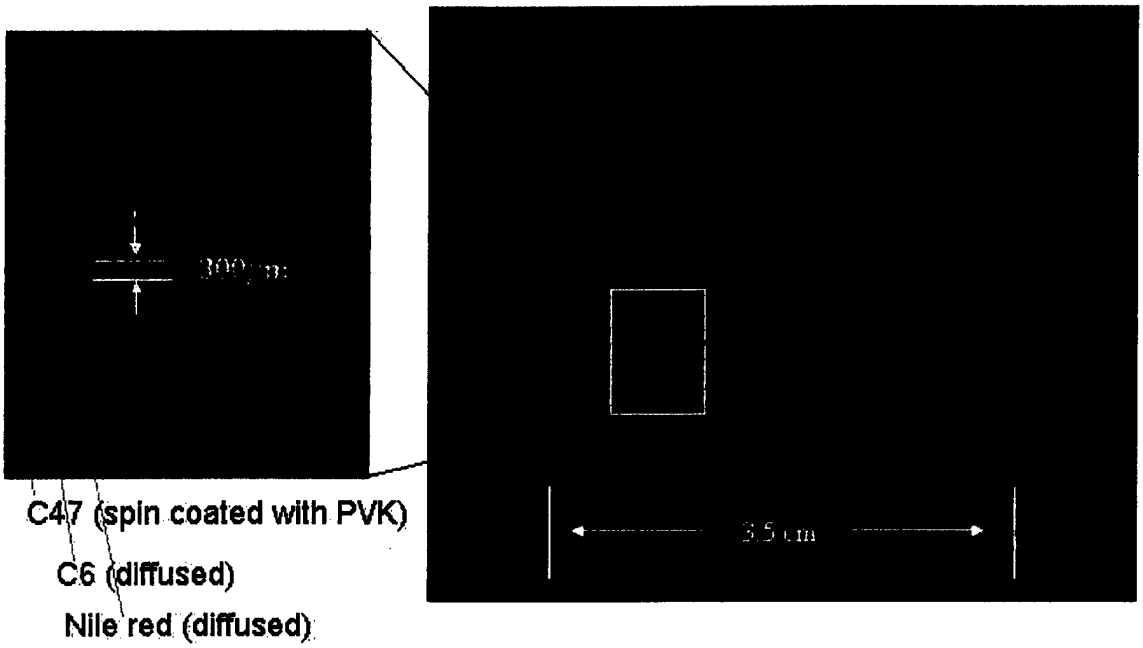


Figure 63. Photoluminescence of dye-doped PVK polymer striped for color pixels after printing and solvent assisted diffusion of C6 (green) and nile Red into a polymer matrix uniformly doped with C47 (blue) [26].

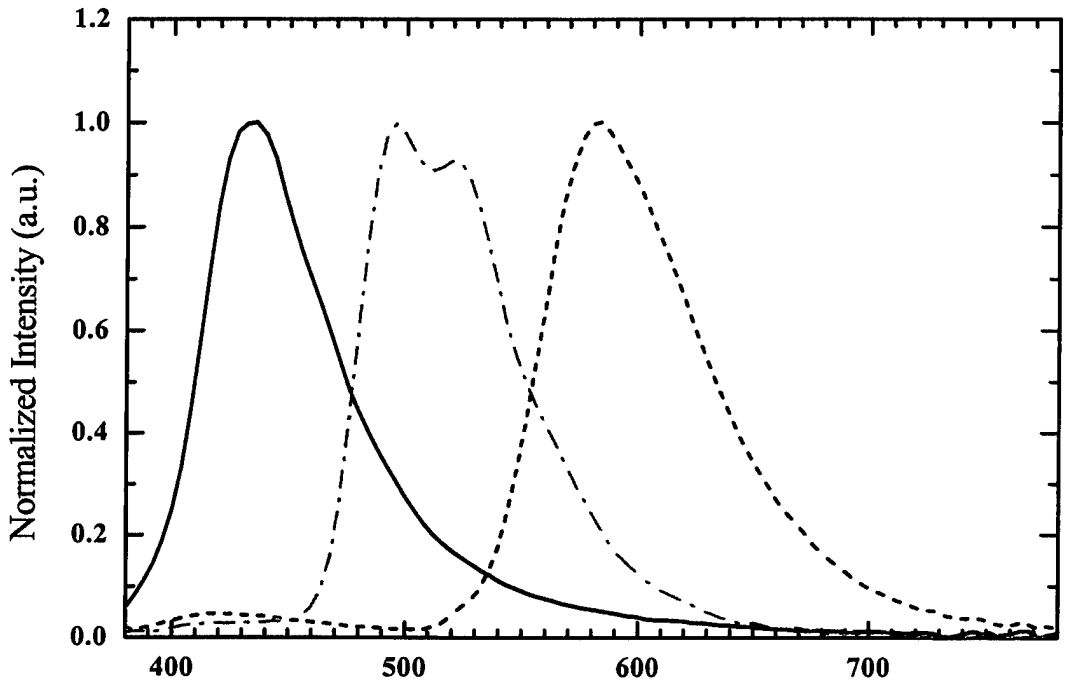


Figure 64. EL emission in RGB pixels using respectively a device polymer of PVK doped uniformly with C47 (blue), with patterned Nile Red, patterned C6, and no added patterned dopant, respectively. [26]

Dry patterned dye transfer: Conclusions and Recommendations

In conclusion, we have demonstrated

-- The basic process of patterned dye diffusion to locally modify the color of OLED's. The process is compatible with large-area manufacturing
-- A process for using "soft masks" for large-area dye diffusion, where the soft masks are applied and removed to the workpiece using lamination
-- A solvent-assisted technique to lower the process temperature by 100 K or more, by adding small amounts of solvent vapor to the ambient during diffusion. Rapid diffusion can be obtained at room temperature.
-- A polymer for a passive matrix display patterned with such a process with RGB emitting stripes with a 300 micron width.

A patent has been applied for the basic process of changing the polymer property by diffusing in dopants after the polymer layer has been formed.

Because this process is "all-dry", it avoids the problems of redistribution of dye or polymer which occur during droplet drying, as occur during ink-jet printing. The soft-mask approaches and anti-stick agents avoid most problems related to damage due to contact. To reduce defects and leakage to yet lower levels, which is especially critical for passive matrices (where one defective pixel can kill an entire row and column), multiplayer structures with blanket layers deposited on top of the doped polymer layers should be investigated. Initial results are very promising. This process depends on several processes which are not fundamentally understood, and thus deserve further investigation. First is the lack of fundamental understanding in the difference between EL and PL when multiple dopants are present. The energy transfer to dye in EL vs. PL should be further investigated. Second, the diffusion of dyes, especially below glass transition temperature and when solvents are present is not predictable from the known literature in a quantitative way. Third, the spatial resolution of the process is not well known. We have demonstrated work on the 100 micron scale, but an immediate technological goal is 10 micron features, as well as the fundamental understanding behind this issue.

The process has the drawback in that a single host material system must be used for all colors, with only dyes adjusting the colors. However, because of its great practical simplicity compared to ink-jet printing in practice, and because the trend of IJP is also to develop a single host material system (for ease of IJP optimization), from a practical point of view this approach is most attractive. Industrial partners for transfer should be developed.

3.2.3 OLED Substrate Patterning: Introduction

A critical figure of merit of OLEDs is the external coupling efficiency (η_{ext}), defined as the ratio of photons externally emitted over photons generated. It is well known that a substantial amount of internally generated light is trapped in the high-index materials of the OLED stack [1], thus reducing η_{ext} to ~0.20-0.30 for typical structures. This commonly reduces the power efficiency of the OLEDs. This is a critical issue since self-heating of OLED displays is predicted to be a possible system limitation.

This report described experimental work and modelling to externally direct more of the generated light. The modelling looks at the question of how much light is trapped in the substrate to begin with in OLED's. It is found that the amount of light is higher than commonly assumed because of the inadequacy of ray optics in modelling OLED's. High index substrates such as plastic are especially attractive for optimizing the emission efficiency.

OLED Substrate Patterning: Approach

The typical OLED consists of a multi-layer sandwich of a planar glass substrate (t_{sub} ~ 1mm, n_{sub} = 1.51, a layer of indium tin oxide (ITO) (t_{ITO} ~ 100 nm, n_{ITO} ~ 1.8), one or more organic layers (t_{org} ~ 0.1 nm, n_{org} = 1.6 - 1.8), and a reflecting cathode (e.g. Mg:Al or Li:Al), where t refers to the layer thickness and n refers to the index of refraction. The coupling efficiency problem in OLEDs is well known and results from light trapping in the high-index materials [1].

This problem can be easily analyzed to first order if microcavity effects are ignored and there is no diffuse scattering at interfaces. This is given just to introduce the problem – later more precise modelling is shown to quantitatively, but not qualitatively, change the results. If all surfaces are planar, light emitted from the back side of the substrate will originate only from light emitted at angles less than the organic-air critical angle, $\theta_{org,\,c1}$, given by $\sin^{-1}(n_{air}/n_{org})$ (ray I in Figure 65). Light emitted at angles larger than $\theta_{org,c1}$, but smaller than the organic-substrate critical angle, $\theta_{org,c2}$, given by $\sin^{-1}(n_{subs}/n_{org})$, are trapped in the substrate (ray II in Figure 65). Light emitted at angles larger than $\theta_{org,c2}$ are trapped in the organic and ITO layers collectively (ray III in Figure 65), and will likely be quickly absorbed by the ITO or at the cathode [2].

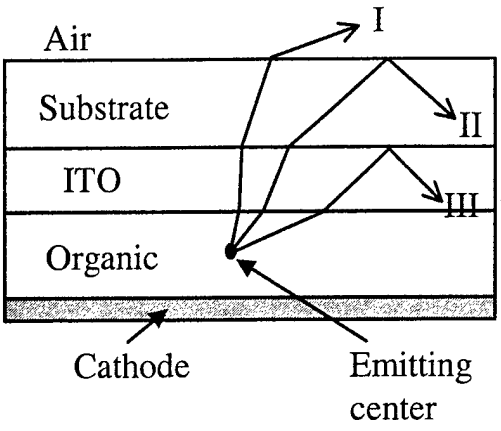


Figure 65. Ray diagrams in planar OLEDs demonstrating loss by light trapping in the substrate (ray II) and in the organic/anode layers (ray III). Only light emitted at sufficiently small angles will escape (ray I).

Assuming the cathode is a perfect reflector, so that light internally reflected towards the cathode and light reflected from the glass-air interface near the critical angle is eventually emitted, and assuming isotropic emission in the organic layer, it is well known that the fraction of generated light escaping from the substrate, $\eta_{cp,ext,pl}$ is [3, 4],

$$\eta_{cp,ext,pl} = \int_0^{\theta_{org,c1}} \sin\theta d\theta = 1 - \cos\theta_{org,c1} \approx \frac{1}{2n_{org}^2}, \tag{1}$$

where the subscript *pl* denotes the case of a planar substrate. The fraction of light trapped in the substrate, $\eta_{cp,subs,pl}$ and in the organic/ITO layers, $\eta_{cp,org}$, are given by,

$$\eta_{cp,subs,pl} = \cos\ \theta_{org,c1} - \cos\ \theta_{org,c2} \tag{2}$$

$$\eta_{cp,org} = \cos\ \theta_{org,c2} \tag{3}$$

Furthermore, the external luminous intensity distribution, where θ_{ff} is the viewing angle in the far-field, under the same assumptions, is given by [5],

$$I_{ext,pl}(\theta_{ff}) = \frac{F}{2\pi} \frac{n_{air}^2 \cos\theta_{ff}}{n_{org}^2 \sqrt{1 - \left(\frac{n_{air}}{n_{org}} \sin\theta_{ff}\right)^2}}, \tag{4}$$

which approximately resembles the cosine intensity profile of a Lambertian emitter. In Eq'n. 4, we assume that all light incident an interface at angles less than the critical angle are completely transmitted (referred to as the T=1 case); one can also calculate $I_{ext,pl}(\theta_{ff})$ assuming that at each angle, some amount of light is reflected (determined by the Fresnel Equations), and that this light is completely lost due to non-ideal cathode reflection, etc... (referred to as the T≠1 case). Both produce similar profiles at small angles, and differ slightly at large angles (see Figure 67(a)).

For glass substrates and typical index of refraction organic layers (e.g. $n_{org} \sim 1.7$), the external coupling efficiency is only ~ 17%. Most internally generated light is thus trapped within the device. The external coupling efficiency has been improved by a factor of 1.9 ± 0.2 by etching grooves in the glass around the OLED to redirect light trapped in the substrate and organic/ITO layers [5]. This method does not lend itself well to the fabrication of device arrays, however, where metal lines and/or circuitry for passive or active matrix drivers would have to cross the deep grooves.

A solution to the light-trapping problem which preserves a planar surface for device processing is to pattern the back side of the substrate in the shape of a sphere with the emitting layer at its center, Figure 66(a). For spherical shapes subtending a large solid angle of emitted rays, light previously trapped in the substrate would be emitted. Not only would the total external efficiency be increased, but because all rays would impinge normally on the substrate-air interface, the normal emitted intensity would also be increased as a result of the reduced refraction. The far field intensity distribution ($I_{ext,sp}(\theta_{ff})$) would then take on the same form as inside the substrate ($I_{subs}(\theta_{subs})$),

$$I_{ext,sp}\left(\theta=\theta_{ff}\right)=I_{subs}\left(\theta=\theta_{subs}\right)=\frac{F}{2\pi}\frac{n_{subs}^2\cos\theta}{n_{org}^2\sqrt{1-\left(\frac{n_{subs}}{n_{org}}\sin\theta\right)^2}}. \qquad (5)$$

This concept has long been known for crystalline semiconductor LEDs [6, 7] and spherical substrate features have previously been used with OLEDs to eliminate microcavity effects, but the effect on external coupling efficiency and the far field emission pattern was not described [2]. As will be shown, by matching the index of the substrate to the index of the emitting material in addition to shaping the substrate, one can potentially eliminate all of the external coupling losses in the device. Increased efficiencies were demonstrated by fabricating OLEDs on glass and polycarbonate (PC) substrates coated with ~100 nm of ITO. The OLEDs were made by spinning on a single poly-(N-vinylcarbazole)(PVK)/2-(4-biphenyl)-5-(4-tert-butylphenyl)-1,3,4-oxadiazole(PBD)/Coumarin 6 (C6) layer, and evaporating a Mg:Ag cathode [8]. The index of refraction of the organic layer was measured to be 1.67 ± 0.01 by ellipsometry at $\lambda = 634$ nm and $\lambda = 830$ nm. The typical device cathode was a circle 1.75 mm in diameter.

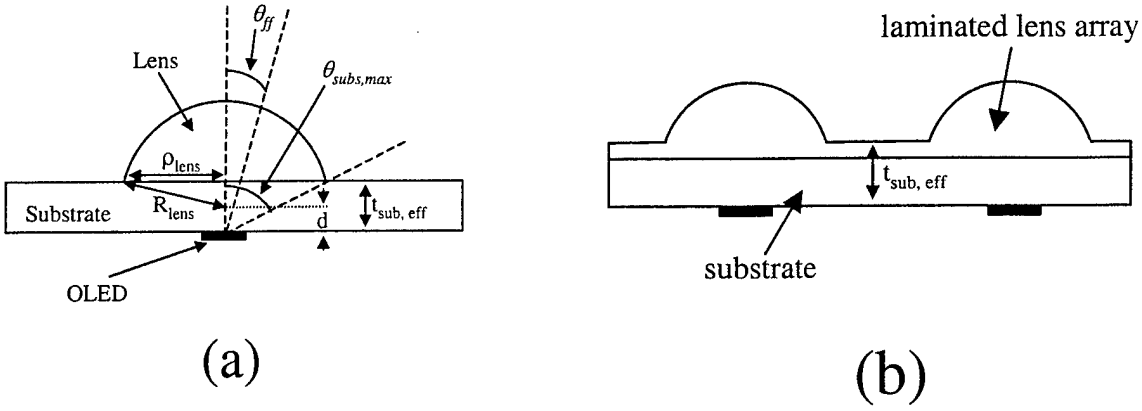


Figure 66. Use of spherical surface features to improve external efficiency. The relevant parameters shown are given for each experimental trial in Table 1. Note that the ray used to define the far-field angle, θ_{ff}, is drawn for the d=0 case, while in the diagram d, the offset between the center of curvature of the lens and the OLED, is drawn as non-zero so that it can be clearly identified. (b) Spherical features implemented as a plastic lens array laminated to a planar substrate. [9]

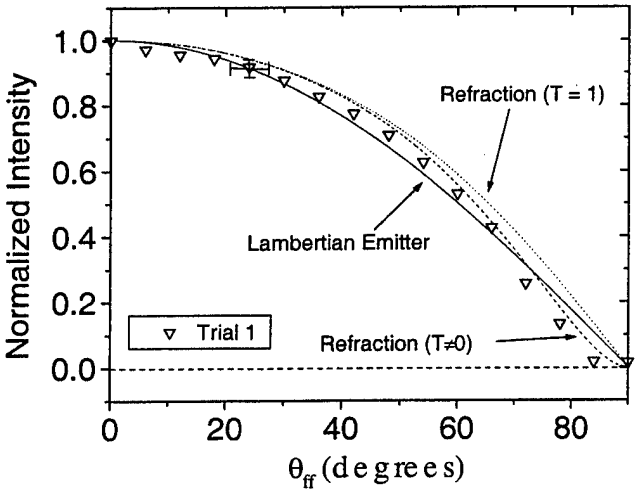
OLED Substrate Patterning: Results and Discussion

Demonstration of Basic Concept and Lamination Approach:

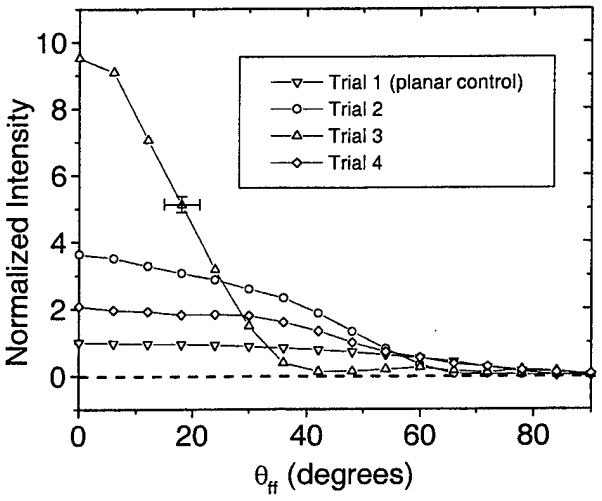
Figure 67(a) shows the far field pattern of a planar device on a glass substrate (see Trial 1 in Table.3.1), along with the expected profile of a Lambertian emitter, and the T=1 (Eqn. (4)) and T≠1 refraction models. Within our uncertainty, each profile reasonably matches the data. In a first experiment (Trial 2), a glass plano-convex lens was attached using an index matching gel to the substrate under an OLED fabricated on planar glass. The far-field pattern in Figure 66(a) was normalized by the normal emitted intensity of the planar device (Trial 1). A clear increase in the normal emission (3.6x) and the total integrated emission (2.0x) (not including edge emission) occurred. Removing the lens and the index matching gel caused the emitted light profile to revert back to its original shape. The sharp peaking of the emission profile (i.e. the increase in the normal emission and the decrease in large-angle emission) occurred because the OLED was slightly below the center of curvature (but still well above the focal point) of the lens, leading to a slight focusing effect. This effect was exaggerated in Trial 3, when the substrate thickness was intentionally increased from 0.7 mm to 2.0 mm. This resulted in an even more highly focused beam, with a nearly 10x increase in normal emitted intensity.

Trial	Substrate Material	Lens Material	R_{lens} (mm)	ρ_{lens} (mm)	$t_{subs,eff}$ (mm)	$\theta_{subs,max}$	d (mm)	I_{normal}/I_0 ± 0.1	F/F_0 ± 0.1
1	Glass (n=1.51)	N/A	N/A	N/A	0.7	N/A	N/A	1.0	1.0
2	Glass (n=1.51)	Glass (n=1.51)	3.4	3.4	0.7	78°	+1.0	3.6	2.0
3	Glass (n=1.51)	Glass (n=1.51)	3.4	3.4	2.0	60°	+2.3	9.5	1.6
4	Glass (n=1.51)	Silicone (n=1.41)	2.7	2.4	1.9	51°	+0.6	2.1	1.6
5	PC (n=1.59)	N/A	N/A	N/A	1.0	N/A	N/A	1.0	1.0
6	PC (n=1.59)	Epoxy (n=1.61)	2.7	2.4	1.0	67°	-0.3	1.6	3.0

Table 4. Substrate and lens parameters (as defined in Fig. 66(a)) for different external coupling experiments. I_{normal}/I_0 and F/F_0 represent the ratio of normal emission intensity and total surface emitted light respectively to the results obtained for identical devices fabricated on planar substrates of the same substrate material. [9]



(a)



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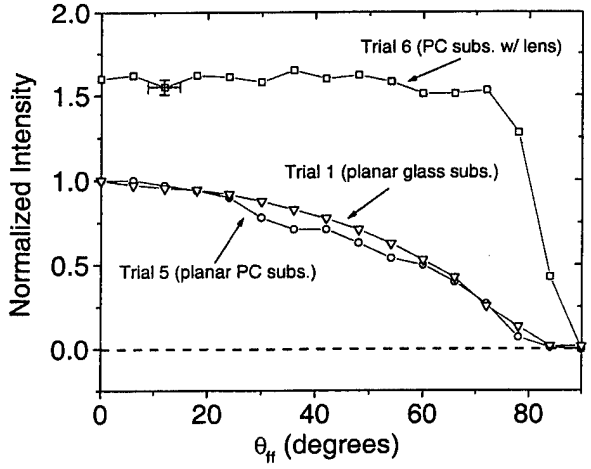

(c)

Figure 67. (a) Measured far field intensity distribution pattern for planar glass substrate and the expected profiles of a Lambertian emitter, and the T=1 (Eqn. (4)) and T≠1 refraction models. (b) Experimental results for glass substrate devices with and without lenses. (c) Experimental results for PC substrate devices with and without lenses, along with the planar glass substrate results. [9]

To demonstrate a practical method for implementing this technique in manufacture, we then created a thin array of transparent microlenses in a molded silicone sheet (n=1.41). This sheet was then laminated to the planar glass substrate after OLED fabrication (Figure 67(b), Trial 4). In this case the center of curvature was closer to the OLED, resulting in a less focused emission profile, with decreased normal emission compared to Trial 2, but larger large-angle emission. The improvement in total emitted light, however, was limited by the relatively small size of the lens we fabricated. The above experiments can at best hope to capture light wave-guided in the substrate, but not the 43% of generated light wave-guided in the organic/ITO layers. To capture this light, high index of refraction substrates must be used. Therefore, devices were made on polycarbonate (PC) substrates (n = 1.59) to reduce the waveguided light in the organic/ITO layers. A planar device had a far-field pattern similar to that for a glass substrate, as expected from Eq'n. (3), which has no dependence on the substrate index (Figure 67(c)). A lens made from molded epoxy (n=1.61) was then applied to the PC substrate. The total emitted intensity was increased by a factor of three. (The data for both the glass and PC substrate planar devices were normalized to their values at 0°, and the data for the epoxy lens on a PC substrate was normalized to the planar PC substrate device at 0°.) The far field intensity profile was extremely flat out to large angles, as expected from an isotropic emitter in the absence of significant surface refraction.

Quantum Mechanical Microcavity Model (QMMCM)

Modelling was carried out to determine how much improvement might be expected and how much light is distributed in different modes I, II and III of Figure 65. Since the layers in a typical OLED are much thinner than the emission wavelength, external coupling of light is poorly described by classical ray optics. The simple equations described above are qualitatively correct in describing what happens to light at different angles of emission, but the quantitative strength of different modes at different angles, assumed to be uniform above, is not correct. A quantum mechanical microcavity theory of OLEDs developed by Bulovic et al. (2) has been used to calculate the distribution of light emission into various modes and to predict the amount of increase in external emission by attaching a lens to the backside of the substrate (10). In this formulation, the exciton is modeled as a radiating dipole, and the external coupling efficiency is proportional to the transition rate given by Fermi's golden rule:

$$f = \frac{2\pi}{h}\sum_{n}\left|\langle m|\boldsymbol{\mu}\cdot\mathbf{E}(\mathbf{k},z)|n\rangle\right|^2\delta(E_n - E_m - h\upsilon) \qquad (6)$$

where $\boldsymbol{\mu}$ is the dipole moment which is assumed to be isotropically distributed, and $\mathbf{E}(\mathbf{k}, z)$ is the electrical field for mode $\mathbf{k}$ at the dipole. E_m and E_n are the energies of the initial and final exciton states. $h\upsilon$ is the energy of the photon emitted. The transition rate is obtained by summing over all $\mathbf{k}$ and υ. The electric field for TE and TM modes at a distance l from the cathode is determined by the microcavity structure:

$$\begin{aligned}\mathbf{E}_{\mathbf{k}}^{TE} &= \mathbf{A}(\mathbf{k})\sin^2(k_{oz}l)\hat{\mathbf{x}} \\ \mathbf{E}_{\mathbf{k}}^{TM} &= \mathbf{B}(\mathbf{k})\cos^2\theta_o\,\mathrm{Sin}^2(k_{oz}l)\hat{\mathbf{y}} + \mathbf{C}(\mathbf{k})\sin^2\theta_o\cos^2(k_{oz}l)\hat{\mathbf{z}}\end{aligned} \qquad (7)$$

where **A(k)**, **B(k)** and **C(k)** are functions of material constants and **k**. k_{oz} is the z component of the wave vector in the emitting layer, and θ_o is the angle of the wave vector in the emitting layer measured from the normal. For spontaneous emission, the electrical fields are normalized such that the energy in each mode is equal to that of a single photon. In our devices (figure 68), the excitons were assumed to be created at the Alq_3/PVK interface and diffuse into Alq_3 with a characteristic length of 20 nm. Two layer devices were used to localize the emission from a known location (the interface), since the vertical location of the emission is a key modelling parameter. The transition rate into each optical mode was computed by integrating over photon energy and exciton location. Energy transfer to the cathode was approximated with the results given by Bulovic et al. (2)., an often overlooked but crucial effect.

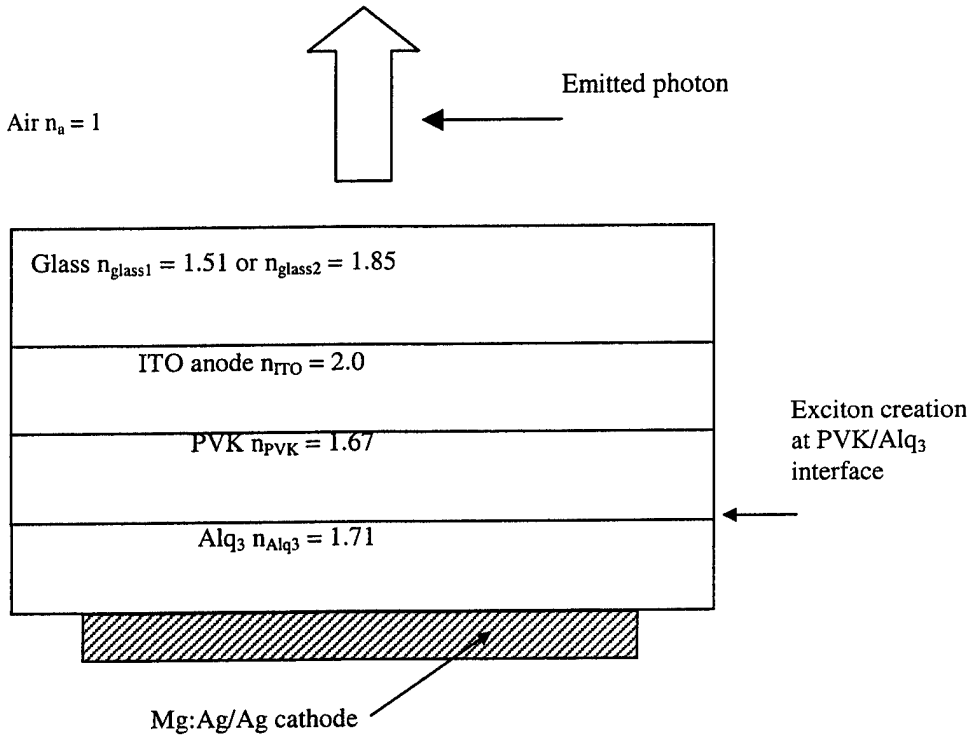

Figure 68. Schematic diagram of OLEDs fabricated on standard (n = 1.51) and high-index (n = 1.85) glass substrates. Excitons are created at the PVK/Alq_3 interface. The location of the emission centers was controlled by the thickness of the Alq_3 layer, which was varied from 20 – 80 nm. External coupling efficiency depends critically on this distance.

The amount of light emitted into external, substrate and ITO/org. modes in OLEDs on either the standard or high-index glass substrates was calculated using the QM microcavity model. Figure 69. shows the detailed distribution of OLEDs with an 80 nm Alq_3 layer on both types of substrates. The external emissions are equal for the two devices, as this fraction is not dependent on the index of refraction of the intervening layers. In the device on high index substrates, light is no longer bounded by TIR at the glass/ITO interface and the ITO/organic modes are eliminated, while these modes remain in the device on standard substrates.

Furthermore, since the thickness of the ITO and organic layers is much less than the wavelength in question, QM effects dominate such that the emission into the ITO/organic modes depends critically on the number of the modes. In our structure, there are at most one TE and one TM mode in the range of the visible wavelengths; therefore, emission into the ITO/organic modes is suppressed. If the ITO and organic layers were thick enough so that the classical limit applies, the total emission would have been equal irrespective of the substrate (dashed part in figure 69).

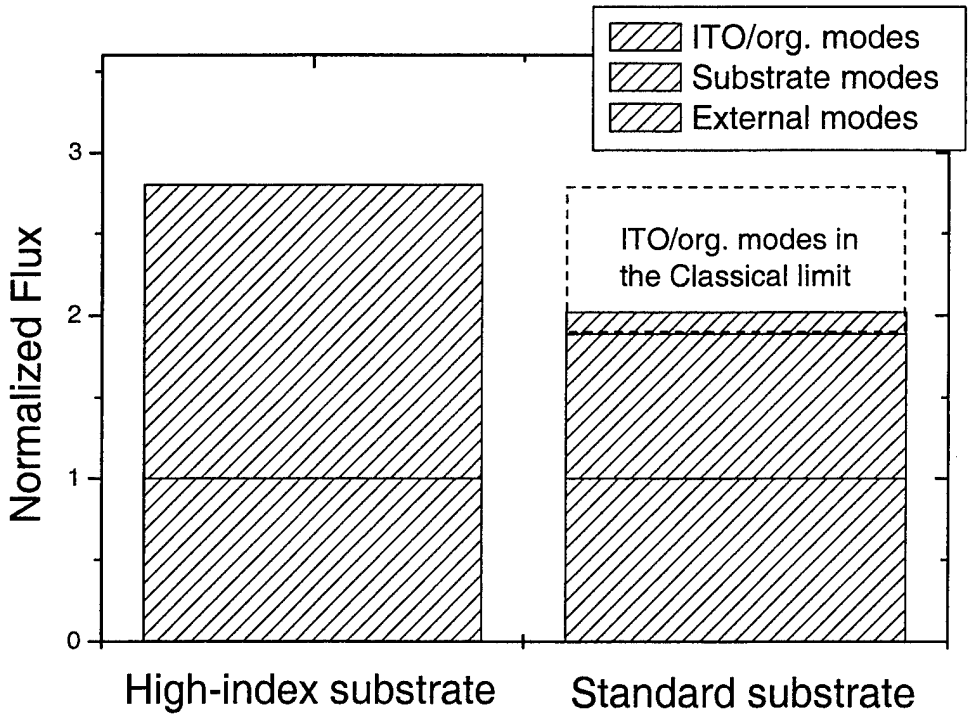

Figure 69. Calculated distribution of emitted light into external, substrate and ITO/organic modes for OLEDs with 80 nm Alq_3, 40 nm PVK and 100 nm ITO on both high-index and standard substrates. ITO/organic modes are eliminated in the case of high-index substrates. In devices on standard substrates, QM effects on the ITO/organic modes lead to a suppression of the total emission rate. [12]

Substrate patterning converts light trapped in the substrate modes into externally emitted light. Consequently, increased emission into substrate modes in OLEDs on high-index substrates allows more light to be harvested via substrate patterning. We calculated the expected increase in the external luminous flux by attaching a lens with the same index as the substrate, assuming a lens large enough that all light previously trapped in the substrate can be emitted externally (Figure 70). The predicted enhancement factor increases monotonically with the index of refraction of the substrate. As the index of the substrate increases beyond that of the emitting layer (n_{Alq3} = 1.71), emission becomes more concentrated in the forward direction due to refraction. Hence there is a larger factor of increase for the luminous flux in the forward 120° cone compared with that in the entire forward half space for higher substrate indices.

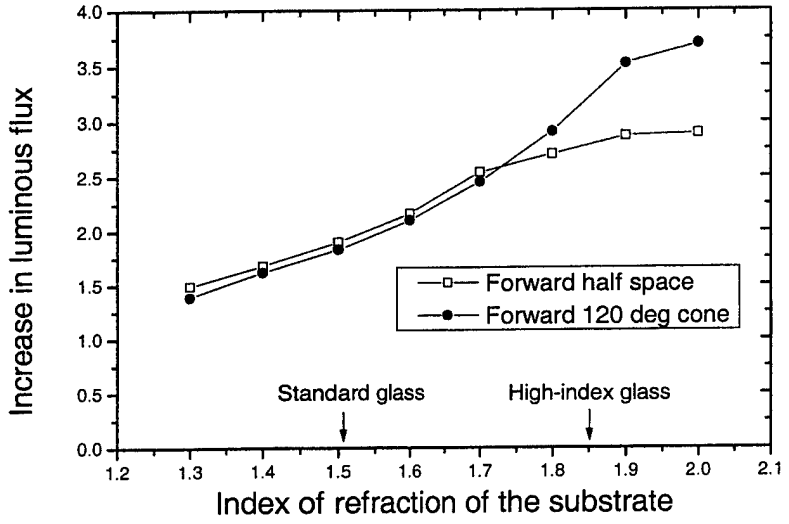

Figure 70. Predicted increases in luminous flux emitted in the forward half plane and the forward 120° cone as a function of the index of refraction of the substrate, assuming complete conversion of substrate modes into external modes.[12.13.15]

Experimental Bi-layer devices with Controlled emission Zone, Plastic and Glass Substrates

Bi-layer OLEDs were fabricated on 0.5 mm-thick soda lime (n_{glass1} = 1.51) and high-index (Schott SF9 glass, n_{glass2} = 1.85) glass substrates. 100 nm of indium-tin-oxide (ITO, n_{ITO} = 2.0) was deposited onto both substrates by RF magnetron sputtering without intentional heating. The sheet resistance of the ITO was 100 Ω/sq, and the transmission was ~80% in the visible. The hole transport layer in all devices was a 40 nm layer of poly-(N-vinylcarbazole) (PVK, n_{PVK} = 1.67), deposited by spin-coating after the ITO surface was treated by an O_2 plasma (8). The electron transport and emitting layer in all devices was tris-(8-hydroxyquinoline)aluminum (Alq_3, n_{Alq} = 1.71), deposited by vacuum sublimation. The cathodes were 30 nm of Mg:Ag (10:1) followed by an Ag cap evaporated through a shadow mask with 0.5 mm-diameter holes. The EL spectrum showed that light emission was exclusively from the Alq_3 layer. The lenses

used in this experiment were made from the same material as the substrates. All lenses have a radius of curvature of 2.0 mm and a height of 1.5 mm, placing the OLED exactly at the center of the curvature. Index matching oil (n_{oil1} = 1.51) and gem refractometer liquid (n_{oil2} = 1.81, both from R.P. Cargille Lab. Inc.) were used to match the lenses to their respective substrates. The far-field emission pattern was measured by a Si photo-detector with a linear polarizer.

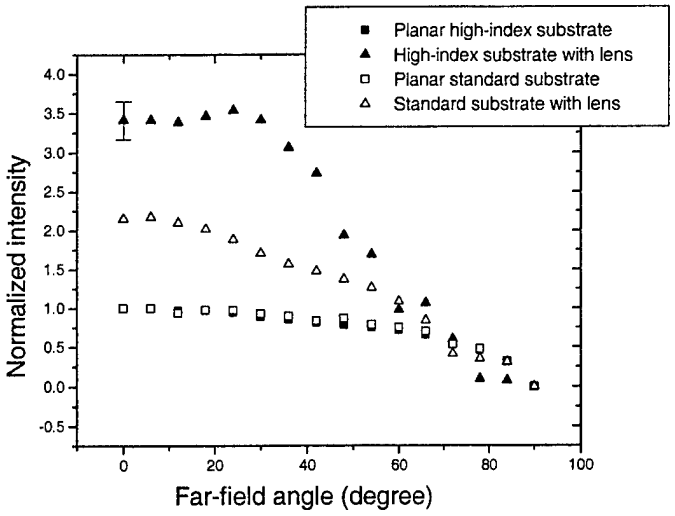

Figure 71. Far-field intensity profile of an OLED (ITO/PVK/Alq_3 (80 nm)/Mg:Ag/Ag) on both high-index and standard glass substrates, before and after lens attachment.[12]

Figure 71. shows the far-field intensity pattern of an OLED with an 80 nm Alq_3 layer on both standard and high-index substrates, with and without a lens attached. As expected, in devices fabricated on planar substrates, the far-field intensity patterns are the same, irrespective of the index of the substrates. Once a lens of the same index as the substrate is attached, the devices on the high-index substrates showed an average increase by a factor of 3.2 in the intensity in the normal direction versus an average increase by a factor of 2.2 for the devices on the standard substrates. These results are very close to the ideal scenario where the OLED is a point source at the center of curvature of the lens where the expected increase is given by n_{glass}^2, i.e., by factors of 3.4 and 2.3 for high-index and standard glass substrates respectively.

When the far-field intensity was integrated to give the total external luminous flux, OLEDs on shaped high-index glass substrates showed significantly larger increases than those on standard glass substrates for all thicknesses of Alq_3 layers examined (20 – 80 nm). Due to microcavity effects, the far-field intensity pattern is not Lambertian. In devices with emission zones close to the cathode (i.e., with a thin Alq_3 layer), in-plane (large mode angle) TM radiation is enhanced with respect to radiation along the normal direction (5). As a result, a larger fraction of light emission suffers from TIR at the glass/air interface and becomes trapped in the substrate.

Consequently, we expect a larger increase in externally emitted light by our substrate mode conversion technique in devices with thinner Alq_3 layers. This is confirmed by our data. The largest such increase observed was in a 20 nm Alq_3 device on high-index substrate, where the external quantum efficiency was increased by a factor of 2.7, versus an increase of 2.2 times for the corresponding device on standard substrates. In OLEDs whose initial quantum efficiencies were optimized by employing a 80 nm Alq_3 layer, shaped high-index substrates increased the external quantum efficiency by a factor of 2.3 versus 1.5 for the corresponding device on standard substrates (Table 4).

Table 5. Summary of increases in luminous flux for OLEDs on standard and high-index substrates after attaching a lens to the backside of the substrate.

	Standard glass		High-index glass	
	Theo.	Expt.	Theo.	Expt.
Q.E. for planar device[a]	N/A	0.35 %	N/A	0.36 %
Flux increase in forward half-space	1.82 X	1.5X	2.62 X	2.3X
Flux increase in forward 120° cone	1.82 X	1.7X	3.20 X	2.9X

[a] Quantum efficiency (external photon/electron) is the same for both types of devices as measured from a group of large-area planar OLEDs.

High-index substrates not only eliminate the ITO/organic modes, but also have a focusing effect on the distribution of emitted light rays. With a large substrate index ($n_{glass2} = 1.85$), diffraction from the emitting layer ($n_{Alq3} = 1.71$) bends light rays forward in the substrate. In the ideal scenario where the OLED is a point source at the center of the curvature of the lens, the far-field intensity pattern in air is identical to the ray distribution in the substrate, so the emission in air is also more concentrated in the normal direction. Thus if we were to look at the light emission in the forward 120° cone, where most of the viewing takes place, the amount of increase in external quantum efficiency is even more remarkable. The observed maximum increase was by a factor of 3.2 for a 20 nm Alq_3 OLED, and a factor of 2.9 for an 80 nm Alq_3 OLED, compared with factors of 2.6 and 1.7 for corresponding devices on standard substrates (Table 4). The discrepancy between theoretical and experimental values can be attributed to the finite size of the OLEDs and the imperfections at the edge of the lenses.

Above we calculated that the external emission amounts to 35.7% of total emission in the OLED on high-index substrates (figure 68), which is much larger than the ~20% commonly assumed (1). To verify this result we correlated the reduction in the substrate-waveguided light with the increase in external emission after the lens was added. This was accomplished by measuring the normal and edge emission simultaneously. Because the ITO/organic modes are

heavily attenuated by the electrodes (5), we assume that the edge emission consists of the substrate-waveguided light exclusively. Further, the total emission rate is assumed to be unchanged from the attachment of a lens on the backside of the substrate. This is reasonable given that the thickness of the substrate, 0.5 mm, was much larger than the wavelength in question. The ratio of emission into the external modes over that into the substrate modes can be calculated from the change in the external and edge emission before and after adding a lens (7). For an OLED with 80 nm Alq_3 on high-index substrate, the data implied an external modes/substrate modes ratio of 0.40 ± 0.08, whereas the ratio in a corresponding device on standard substrate was found to be 1.30 ± 0.30. From the calculations presented in figure 3 we expect this ratio to be 0.56 and 1.12 for devices on high-index and standard substrates respectively, so the agreement between theory and experiment is very good considering the large error associated with the measurement. [12. 13. 15]

Increased light emission into the substrate modes can be further demonstrated by a more practical substrate modification technique. When OLEDs were fabricated on substrates whose backsides were roughened by abrasion (resulting RMS roughness = 75 nm in both cases as measured by a profilometer). Light in the substrate modes was partially scattered forward. Figure 72 shows the far-field intensity profile of the resulting OLEDs. The OLED on the high-index substrate exhibited a 39% increase in total external emission compared with a 17% increase for the OLED on the standard substrate. Again, this is consistent with the numerical results presented in figure 69, where emission into substrate modes in the device on high-index substrates is roughly twice that of the corresponding device on standard substrates.

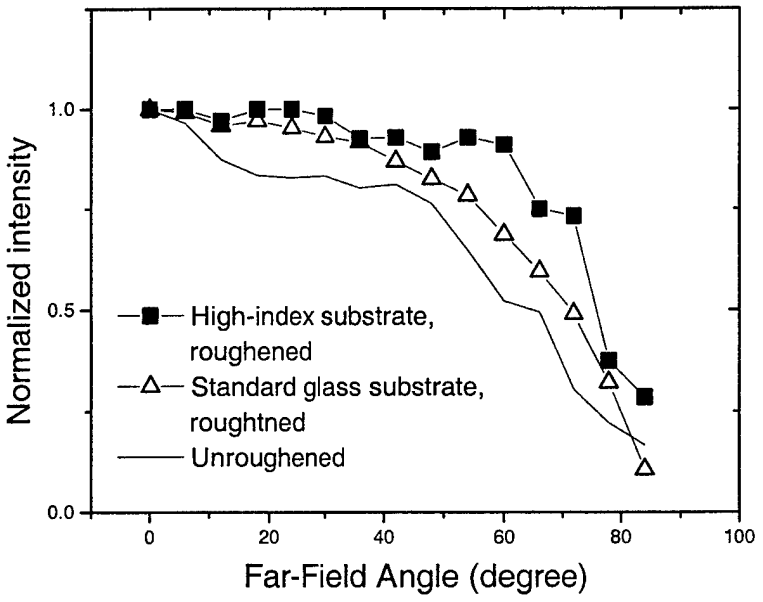

Figure 72. Far-field intensity of OLEDs with roughened backside. Total luminous flux from the OLED on a high-index substrate was increased by 39% as compared with the unroughened sample; the increase for the OLED on a standard glass substrate was only 17%. Roughening the backside does not change the intensity in the normal direction. [12]

OLED Substrate Patterning: Conclusions and Recommendations

A technique for increasing the total emitted efficiency of an OLED by at least a factor of three has been demonstrated with the patterning of features on the back of the substrate. To achieve maximum impact, one must not only capture light wave-guided in the substrate, but also light wave-guided in the organic/ITO layers, which we accomplished by using high-index transparent substrates. By adjusting the location of the center of curvature of the surface features, and the shape of the feature, the far-field emission pattern can be tuned. Lamination of molded or stamped plastic lens arrays is an attractive option for manufacturing, especially compared to standard lithography and etching approaches.

The work done in this work was done on isolated devices. Adding backside surface features will probably "mix" the light emitted by adjacent pixels especially when the pixel separation is small compared to the substrate thickness. The method will then be most attractive when thin substrates, such as flexible plastic, is used. Thus further work is needed on examining how this method should be used for a pixilated display. It is possible that a flexible thin plastic display will fundamentally have higher efficiency than one fabricated on conventional glass.

The optical modelling tool (Quantum Mechanical Microcavity Model) which has been developed as part of this work is a very valuable tool. It incorporates (a) the two main effects which control the efficiency of exciton emission into external modes (cathode quenching [15]) and (b) the microcavity effects into various substrate modes. It can be used to trace the various efficiency loss mechanisms in both planar and shaped strucutures. It has already been transferred to Universal Display Corporation where it is currently being used to design high efficiency structures. The tool should further be used to look at tradeoffs as a function of the non-radiative lifetime of the emitting center. Initial indications are that different structures should be used to optimize the external coupling when centers with low or high radiative efficiencies are used [15].

3.3 Organic Thin Film Transistors and Circuits – Jackson (Penn State)

3.3.1 Pentacene OTFT Polymer Substrate Device Fabrication

Although roll-to-roll processing would be attractive for manufacturing scale OTFT display fabrication, for simplicity polyethylene naphthalate (PEN) substrates were mounted to glass carriers for this work. Prior to mounting the PEN substrates were pre-shrunk at 150 °C for two hours. After substrate mounting, indium-tin oxide (ITO) pixel electrodes, nickel gate electrodes, a silicon dioxide gate dielectric layer, and palladium source and drain contacts were all deposited by ion-beam sputtering and patterned by photolithography and lift-off. Before pentacene active layer deposition the silicon dioxide gate dielectric was vapor treated with octadecyltrichlorosilane to improve device performance. Pentacene was deposited by thermal evaporation with a deposition rate near 0.5 Å/s and with the substrates held at 60 °C. Prior to the active-layer deposition, the pentacene was purified by temperature-gradient vacuum sublimation.

Because pentacene, like many organic semiconductors, is degraded by exposure to most common solvents, an aqueous-based photolithographic process was used to pattern the pentacene active layers. A thin layer of polyvinyl alcohol (PVA) photosensitized with chromium was applied to the pentacene active layer by spin casting. The device active area is exposed to UV light through a mask (as in conventional photolithography) and the unexposed PVA is removed by development in water. The patterned PVA is then used as a mask to pattern the pentacene active layer using an oxygen plasma.

Results

The process described above has a maximum process temperature of 110 °C after the pre-shrink step. Using this process we have fabricated pentacene OTFTs on PEN substrates with field-effect mobility as large as about 2 cm^2/V-s. Typical mobility is 0.5 – 1 cm^2/V-s with on/off current ratio, subthreshold slope, and threshold voltage acceptable for display and circuit fabrication. In addition, the available current drive is sufficiently large that these OTFTs can easily serve as the drive transistor for active matrix OLED displays.

Figure.73a shows an OTFT pixel with the TFT electrodes labeled and a section of a pixel array. Figure 73b shows a completed PEN substrate with pentacene OTFT devices and circuits. The substrate also has several small polymer dispersed liquid crystal (PLDC) test displays (the milky area is the PLDC material sandwiched between the bottom PEN active substrate and an ITO coated mylar top substrate). The PLDC allows a simple reflective display and avoid problems with plastic substrate birefringence.

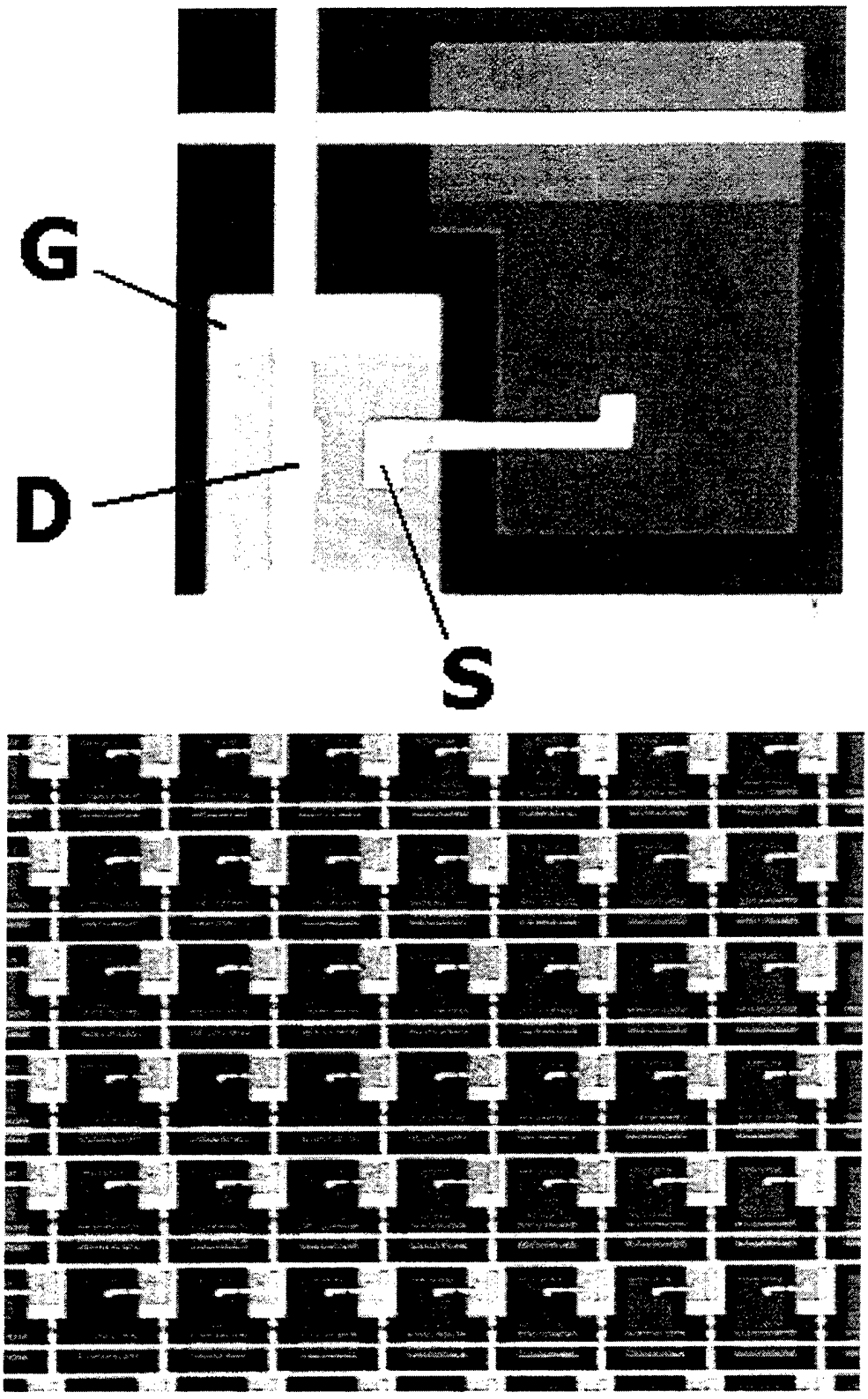

Figure 73a. OTFT single pixel and pixel array section fabricated on polymeric substrate.

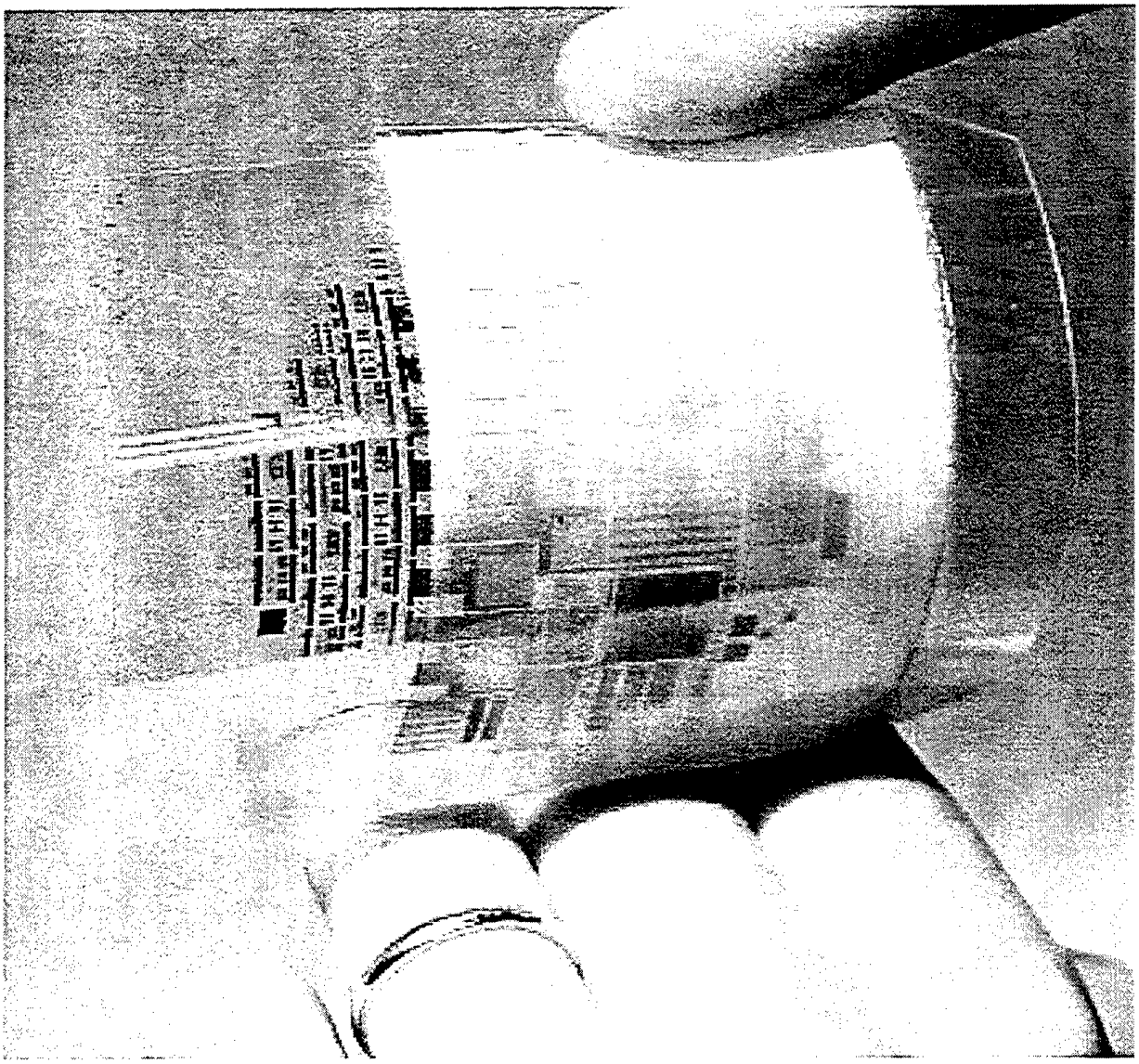

Figure 73b. PEN OTFT substrate with devices, circuits and PDLC test displays.

3.3.2 Napthacene OTFTs

We have also fabricated organic thin film transistors (OTFTs) using the small-molecule organic semiconductor naphthacene as the active layer material. Napthacene OTFTs have field-effect mobility greater than 0.1 cm^2/V-s, in the range useful for several large-area electronic applications. OTFTs fabricated using naphthacene films show a large photosensitivity; of potential interest for applications requiring phototransistors. The subthreshold region electrical characteristics of naphthacene OTFTs allow the fabrication of OTFT circuits without active layer patterning or the use of a level shift stage such as that used to fabricate pentacene OTFT circuits. 5-stage ring oscillators fabricated with naphthacene OTFTs have single-stage propagation delay of less than 28 μs; the fastest organic circuits reported to date.

In this work we investigated naphthacene, a homologue of pentacene, for use as the active layer material in OTFTs. Previous reports of naphthacene OTFTs list no observed field-effect (7). Recently however high mobility organic transistors and injection lasers based on naphthacene single crystals have been reported (8,9). We report here on OTFTs fabricated using thermally-evaporated polycrystalline naphthacene thin films with performance in the range of interest for some large-area electronic applications and with functionality currently not available with pentacene.

For convenience we fabricated napthacene test OTFTs on heavily-doped thermally-oxidized single-crystal silicon substrates. The heavily-doped silicon provides a convenient substrate and gate contact. The thermally-grown silicon dioxide layer provides a high quality gate insulator. Palladium source and drain contacts were deposited by ion beam sputter deposition and patterned using photolithography and a lift-off process. Prior to the active layer deposition we chemically-modified the silicon dioxide gate dielectric using the silane coupling agent octadecyltrichlorosilane (OTS). We find OTS treatment can improve field-effect mobility, subthreshold slope, and threshold voltage. The patterned substrates are treated with OTS using a vacuum vapor prime technique. Following the gate insulator treatment, a 50 nm thick naphthacene film was deposited by thermal evaporation to complete the OTFTs. The naphthacene active layer material was purchased from a commercial source and further purified by temperature gradient vacuum sublimation.

Device Characterization

Electrical measurements were made on the naphthacene OTFTs that were fabricated as described previously. Discrete devices and circuits were characterized in a nitrogen ambient glovebox and using a Hewlett Packard HP4156B Semiconductor Parameter Analyzer, Oscilloscope, and DC power supply. Figure 74a shows the electrical characteristics of a naphthacene OTFT with and without illumination. The OTFT has a channel width of 220 μm and channel length of 10 μm. The silicon dioxide gate dielectric has a thickness of 300 nm.

Figure 74b shows a plot of the square root of drain current as a function of gate-to-source voltage for the OTFT with and without illumination. The OTFT is biased in the saturation region of operation with a drain-to-source voltage of –40 V. The drain current obeys a square-law relationship as expected for a field-effect transistor. We extract a field-effect mobility of

0.12 cm^2/V-s from the slope of the straight-line portion of the curve and a threshold voltage of -3 V with no illumination. With illumination the extracted field-effect mobility is near 0.07 cm^2/V-s and the threshold voltage shifts to a positive value of 14 V.

Figure 74c shows a plot of drain current as function of gate-to-source voltage for the OTFT biased in the saturation region of operation with a drain-to-source voltage of –40 V. A large change in current is seen in the subthreshold region of device operation with illumination showing the strong photosensitivity of naphthacene OTFTs with common microscope light illumination. For some range of gate bias the light induced current modulation ratio is as large as 10^5.

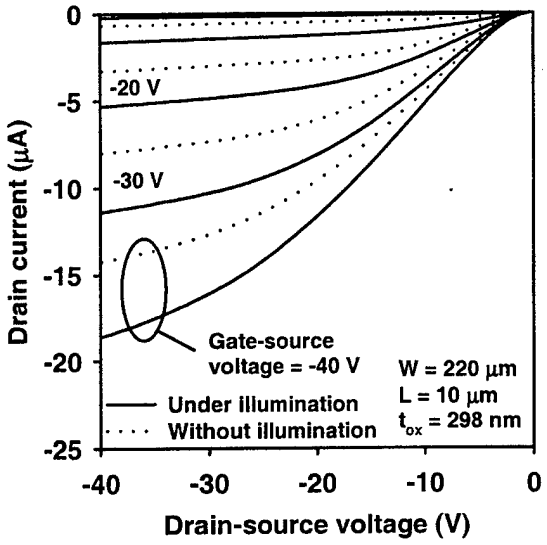

Figure74a. Characteristics.

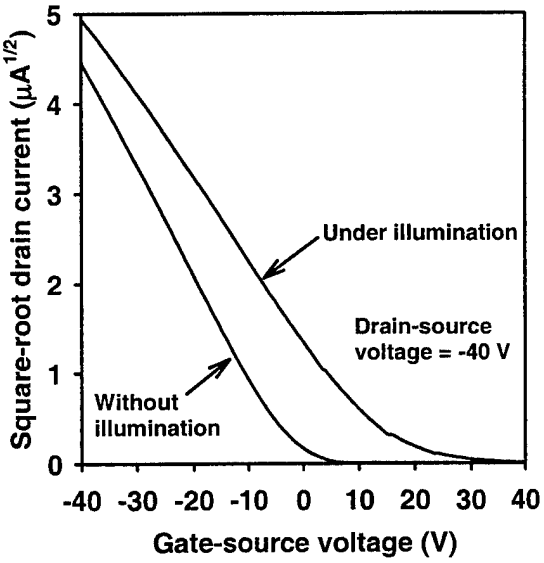

Figure74b. Square root of drain current plot with and without light.

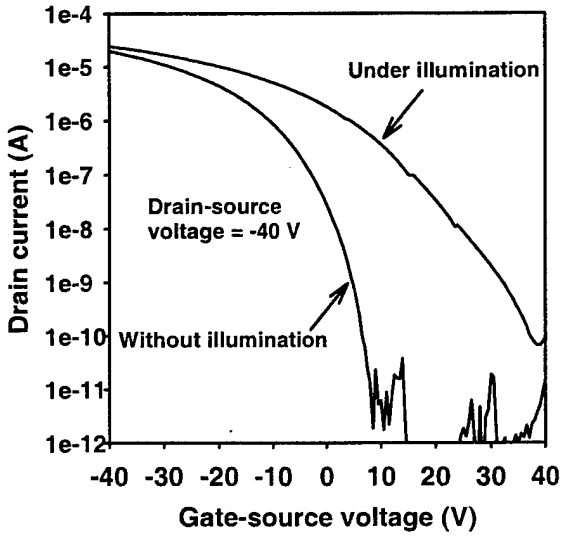

Figure 74c. Changes in subthreshold region with and without light.

Such photosensitivity is common for several small-molecule organic semiconductors and has been the topic of research for several decades where typically single crystals of such materials have been used to fabricate diode structures (10). The large change in electrical characteristics with microscope illumination for OTFTs reported here is likely due to trap filling. The position of the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) with reference to the vacuum level and the separation between levels favor the formation of deep trapping states. Such trapping states can be expected from the structural imperfections at grain boundaries and within grains for these thermally evaporated polycrystalline naphthacene thin films. No attempt was made to quantify the position and density of such states using sub-gap illumination or other techniques. However the effect of such trapping states on carrier field-effect mobility, subthreshold region characteristics, and threshold voltage has recently been reported for organic transistors (11). The large photosensitivity may be useful for bistable and other active pixel circuits.

Naphthacene OTFT Circuits Results

To fabricate naphthacene OTFTs with patterned gate electrodes and gate dielectric for use in circuits we used the device structure shown in Figure 74d with ion beam deposited and patterned nickel gate electrodes (50 nm) and silicon dioxide gate dielectric (257 nm). Such a device structure has been reported on elsewhere and used to fabricate pentacene OTFTs and OTFT circuits on glass and polymeric substrates. For convenience, oxidized silicon wafers were again used as substrates. Following the gate electrode and dielectric deposition and patterning, discrete OTFTs and OTFT circuits were completed using the process described previously.

To measure the speed of circuits based on naphthacene OTFTs we fabricated 5-stage ring oscillators. Figure 74e shows an optical micrograph of a 5-stage ring oscillator with output buffer stage. Figure 74f shows the AC-coupled output for a 5-stage ring oscillator with single stage propagation delay as low as 28.5 μsec biased at –60 V. Propagation delay was found to be dependent on illumination; with circuits under illumination operating significantly faster than circuits biased at the same operating voltage but without illumination.

The operation of naphthacene OTFT circuits is unlike pentacene OTFTs which operate as slightly depletion mode devices and require active layer patterning to reduce current leakage in the un-gated field regions and the use of a level shift stage to offset the output voltage to a useable input level. Naphthacene ring oscillators do not require either patterning of the active layer or level shifting of the output voltage to achieve stable oscillation. Patterning of small-molecule active layer materials has proven difficult, greatly complicating device fabrication and circuit design. Devices such as those based on naphthacene thin films greatly simplify device processing and circuit design.

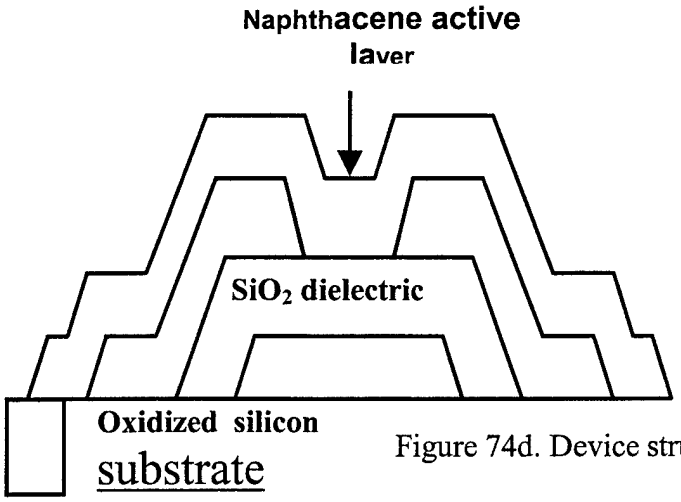

Figure 74d. Device structure.

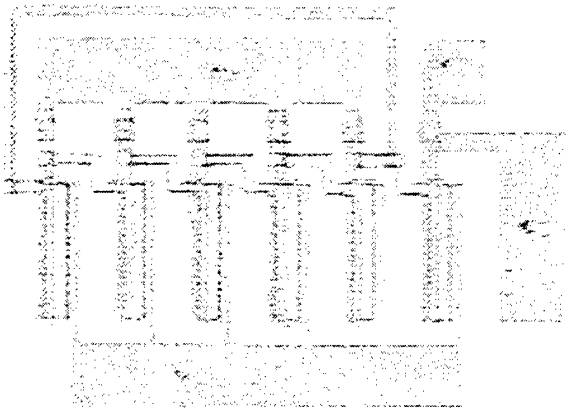

Figure74e. Optical micrograph

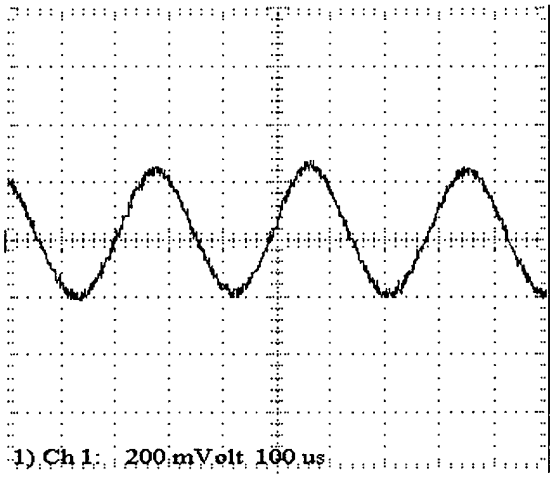

Figure74f. Oscillator output

Napthacene OTFT Summary

We have fabricated naphthacene OTFTs and OTFT circuits with electrical characteristics that show a large photosensitivity; possibly of interest for thin film electronicn applications. Discrete OTFTs have field-effect mobility greater than 0.1 cm^2/V-s, low subthreshold slope, large on/off current ratio and near zero threshold voltage. Although the field-effect mobility of naphthacene OTFTs is an order of magnitude lower than demonstrated for OTFTs fabricated using the best pentacene thin films, OTFT circuits fabricated using naphthacene films operate at speeds that are 25% faster than pentacene OTFT circuits. Such improvement is the result of improved subthreshold region characteristics allowing the fabrication of circuits without the use of level shift stages which significantly limits circuit speed. To our best knowledge these are the fastest organic thin film transistor circuits reported and among the first reports of organic thin film phototransistors.

Future Directions

The low temperatures and simple processing required for OTFT devices and circuits allows fabrication on arbitrary substrates. Fig. 75 shows simple OTFTs fabricated on a key ring and on a piece of a cotton-polyester bed sheet. These and related results [1-6] point to the possibility of fabricating displays and thin film electronics anywhere.

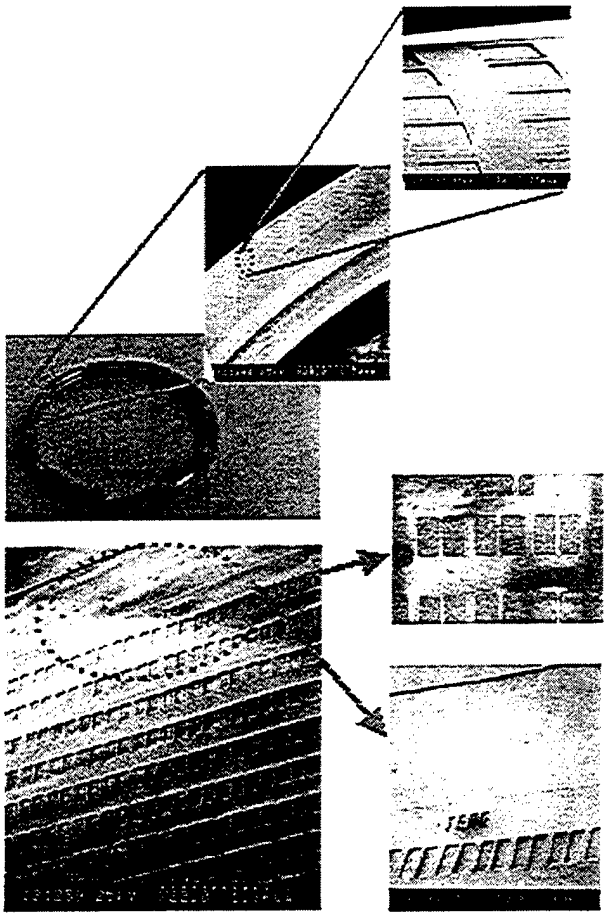

Figure 75. OTFTs fabricated on a key ring and bed sheeting.

4. CONCLUSIONS AND RECOMMENDATIONS

Low processing Temperature Dielectrics for Plastic Substrates

As noted, we found PECVD TMS oxide thin films deposited at these temperatures and pressures exhibit adjustable stress. The type of stress, including tensile stress, zero stress, and compressive stress, as well as the stress level can be tailored as desired by changing the deposition conditions and film thickness. In addition, the conformality of PECVD TMS oxide thin films was found to vary significantly with the deposition conditions. It improves when the deposition pressure is raised and the substrate temperature is reduced. The mechanisms for the variations of stress and conformality with respect to deposition conditions are discussed in this study. The adjustable stress and conformality of the PECVD TMS oxide make it a promising material for many low temperature applications such as inter-level dielectric, planarization, micro-electro-mechanical systems (MEMs) fabrication, and encapsulation.

Direct Deposition onto Plastic--Micro-crystalline Si TFTs

This work shows the promise of the HDP approach for directly depositing silicon onto plastics for all low-temperature processing silicon TFTs. Although the microcrystalline silicon thin film transistors we produced have been fabricated on glass substrates at low temperatures (<285 °C) using an ECR high-density plasma source, clearly the temperatures used are compatible with many plastics.. The deposition rates for n-type doped silicon, silicon dioxide, and intrinsic silicon layers were all in the range of 120 - 150 Å/min. This whole TFT fabrication procedure used only two masks and one alignment and no critical etch step was involved. When annealed at 340 °C mc-Si TFT has linear field effect mobility of 12 cm^2/V-s, on/off current ratio of $\sim 10^6$, off-current of $\sim 4x10^{-13}$ A/ m, and threshold voltage of 5V.

Clearly this is a viable approach to Si TFT fabrication on plastic that can be fully developed. The steps we believe need further work principally involve stress control and plastic deformation problems impacting lithography. We believe the best approach to addressing these problems is to side-step them and move to a separation-based approach as discussed in the next section. This side-steps dimensional integrity issues on plastics and allows truly high performance silicon TFTs to be on plastic. This can be acheived since high processing temperatures can be used in the TFT fabrication before the TFTs are transferred to their flexible, plastic substrate.

Jet Printing

We have developed a system to investigate the dye doping by IJP of polymer OLED's, including a highly controllable all-glass ink jet printer and digital imaging equipment for studying IJP droplet formation and droplet drying phenomena. Using a very low vapor pressure solvent, uniform dye distribution over the droplet area was achieved. The dye distribution is critically affected by the dynamics of the drying process, which at present are only qualitatively understood. Integrated 250-micron RGB devices were demonstrated with good color uniformity and with electrical properties comparable to spin-coated devices without IJP.

This work shows that ink-jet printing can fundamentally be used for OLED manufacturing. However, the results depend critically on the organic material system and the exact details of the printer, due to requirements for stable droplet formation and due to the drying dynamics of the solvent/organic mixture. The critical issue is to assure a uniform profile across the pixel. There are two recommendations. First, the droplet drying process is not fundamentally understood, so further science in this area is required, especially in complicated prepatterned structures as would be used in real devices. Second, to realistically address the problems of drying profile and droplet formation for a production environment, joint work between the display system manufacturer, organic materials supplier (OLED materials expert), and the printing tool company will be required.

Patterned dye transfer

In conclusion, we have demonstrated

-- The basic process of patterned dye diffusion to locally modify the color of OLED's. The process is compatible with large-area manufacturing
-- A process for using "soft masks" for large-area dye diffusion, where the soft masks are applied and removed to the workpiece using lamination
-- A solvent-assisted technique to lower the process temperature by 100 K or more, by adding small amounts of solvent vapor to the ambient during diffusion. Rapid diffusion can be obtained at room temperature.
-- A polymer for a passive matrix display patterned with such a process with RGB emitting stripes with a 300 micron width. A patent has been applied for the basic process of changing the polymer property by diffusing in dopants after the polymer layer has been formed.

Because this process is "all-dry", it avoids the problems of redistribution of dye or polymer which occur during droplet drying, as occur during ink-jet printing. The soft-mask approaches and anti-stick agents avoid most problems related to damage due to contact. To reduce defects and leakage to yet lower levels, which is especially critical for passive matrices (where one defective pixel can kill an entire row and column), multiplayer structures with blanket layers deposited on top of the doped polymer layers should be investigated. Initial results are very promising. This process depends on several processes which are not fundamentally understood, and thus deserve further investigation. First is the lack of fundamental understanding in the difference between EL and PL when multiple dopants are present. The energy transfer to dye in EL vs. PL should be further investigated. Second, the diffusion of dyes, especially below glass transition temperature and when solvents are present is not predictable from the known literature in a quantitative way. Third, the spatial resolution of the process is not well known. We have demonstrated work on the 100 micron scale, but an immediate technological goal is 10 micron features, as well as the fundamental understanding behind this issue. The process has the drawback in that a single host material system must be used for all colors, with only dyes adjusting the colors. However, because of its great practical simplicity compared to ink-jet printing in practice, and because the trend of IJP is also to develop a single host material system (for ease of IJP optimization), from a practical point of view this approach is most attractive. Industrial partners for transfer should be developed.

Substrate Patterning

A technique for increasing the total emitted efficiency of an OLED by at least a factor of three has been demonstrated with the patterning of features on the back of the substrate. To achieve maximum impact, one must not only capture light wave-guided in the substrate, but also light wave-guided in the organic/ITO layers, which we accomplished by using high-index transparent substrates. By adjusting the location of the center of curvature of the surface features, and the shape of the feature, the far-field emission pattern can be tuned. Lamination of molded or stamped plastic lens arrays is an attractive option for manufacturing, especially compared to standard lithography and etching approaches. The work done in this work was done on isolated devices. Adding backside surface features will probably "mix" the light emitted by adjacent pixels especially when the pixel separation is small compared to the substrate thickness. The method will then be most attractive when thin substrates, such as flexible plastic, are used. Thus further work on examining how this method should be used for a pixilated display It is possible that a flexible thin plastic display will fundamentally have higher efficiency than one fabricated on conventional glasss.

Future Directions

The low temperatures and simple processing required for OTFT devices and circuits allows fabrication on arbitrary substrates. Figure 75 shows simple OTFTs fabricated on a key ring and on a piece of a cotton-polyester bed sheet. These and related results [1-6] point to the possibility of fabricating displays and thin film electronics anywhere.

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APPENDIX A
PATENTS PRODUCED UNDER THIS PROGRAM

Fonash Group Patents

"Metal-Contact Induced crystallization in Semiconductor Devices"
Inventors: Fonash; Stephen (University Park, PA); Bae; Sanghoon (University Park, PA)
Assignee: The Trustees of Pennsylvania State Univeristy (University Park, PA)
Application No.: 09/400,496 filed September 21, 1999
U.S. Patent No.: 6.277.714

"Electrostatic Printing of Metallic Toner to Produce a Polycrystalline Semiconductor from and Amorphorphous Semiconductor"
Inventors: Fonash; Stephen (University Park, PA); Kalkan; Kaan (University Park, PA); Detig; Bob
Assignee: The Trustees of Pennsylvania State Univeristy (University Park, PA)
Application No.: 09/340,009 filed May 25, 1999
U.S. Patent No.: 6,171,740

"Methods for Modifying Solid Phase Crystallization Kinectics for A-Si Films"
Inventors: Fonash; Stephen (University Park, PA); Bae; Sanghoon (University Park, PA); Reese; Kinji
Assignee: The Trustees of Pennsylvania State Univeristy (University Park, PA)
Application No.: 08/835,695 filed April 10,1997
U.S. Patent No.: 6,165,875

"Low Temperature, High quality Silicon Dioxide Thin Films Deposited Using Tetramethylsilane (TMS)"
Inventors: Fonash; Stephen (University Park, PA); Reber; Douglas M.
Assignee: The Trustees of Pennsylvania State Univeristy (University Park, PA)
Application No.: 09/110,923 filed July 6, 1998
U.S. Patent No.: 6,159,559

"High Conductivity Thin Film Material For Semiconductor Devices"
Inventors: Fonash; Stephen (University Park, PA); Kakkad; Ramesh
Assignee: The Trustees of Pennsylvania State Univeristy (University Park, PA)
Application No.: filed:August 15,1994
U.S. Patent No.: 6,013,565

Wagner Group Patents

Electrophotographic Patterning of Thin Film Circuits"
Inventors: Gleskova, Helena (Princeton, NJ); Shen, Dashen (Madison, AL); Wagner, Sigurd (Princeton, NJ)
Assignee: The Trustees of Princeton University (Princeton, NJ)
Application No. 08/621,582 filed March 26, 1996
US patent 6,080,606, issued June 27, 2000

"Material and Method for Printing High Conductivity Electrical Conductors and Other Components of Thin Film Transistor Arrays"
Inventors: Kydd, Paul H. (Lawrenceville, NJ); Wagner, Sigurd (Princeton, NJ); Gleskova, Helena (Princeton, NJ)
Assignee: Parelec, Inc, (Rocky Hill, NJ)
Application No. 09/468/649 filed December 21, 1999
US patent number 6, 274, 412 B1, issued August 14, 2001

Sturm Group Patents

"Fabrication of Organic Semiconductor Devices Using Ink-Jet Printing,"
Inventors: Sturm; James C.(Princeton, NJ); Wu; Chung Chih (Taipai, TW), Marcy, Duane (Ewing, NJ), and Hebner, Thomas R.(Princeton, NJ)
Assignee: The Trustees of Princeton University (Princeton, NJ)
Application No.: 238708 filed Jan 28, 1999
US Patent 6,087,196 issued July 11, 2000.

"Plasma treatment of conductive layers"
Inventors: Sturm; James C. (Princeton, NJ); Wu; Chung-Chih (Taipei, TW)
Assignee: The Trustees of Princeton University (Princeton, NJ)
Application No. 202152 filed May 5, 1999
US Patent 6,259,202

"Micro-mechanical probes for charge sensing"
Inventors: Sturm; James C. (Skillman, NJ); Pangal; Kiran (Princeton, NJ); Firebaugh; Samara L. (Cambridge, MA)
Assignee: The Trustees of Princeton University (Princeton, NJ)
Application No.: 873819 filed June 12, 1997
US Patent 6,300,756

"Modification of Polymer Optoelectronic Properties after Film Formation by Impurity Addition or Removal"
Inventors: Sturm, James C. (Princeton, NJ), Hebner, Thomas, and Pschenitzka, Florian (Princeton, NJ);
Application No. 09/673204 filed Feb. 1, 2001
Patent Pending

Jackson Group Patents

"a-Sio:H TFT/Organic TFT Complementary Circuits"
Inventors: Jackson, Thomas N. (University Park, PA), et Al.
Assignee: The Trustees of Pennsylvania State University (University Park, PA)
Application No.: 60/089,830 filed June 19,1998
US Patent 09/485,847

"Dip-Coating Technique for Fabricating Polymeric Thin Films with Improved Ordered Structure"
Inventors: Jackson, Thomas N. (University Park, PA), et Al.
Assignee: The Trustees of Pennsylvania State University (University Park, PA)
Application No09/450,991 filed November 29,1999
Patent Pending

"Modification of Drain-Source Contacts of OTFTS by Self-Assembled Monolater of Charge Transfer Agent"
Inventors: Jackson, Thomas N. (University Park, PA), et Al.
Assignee: The Trustees of Pennsylvania State University (University Park, PA)
Application No.: 09/763,948 filed March 28,2001
Patent Pending

"Development of Copolymer of 3-Methyl thiophene and 3-Hexyl thiophene for Organic Thin Film Transistors"
Inventors: Jackson, Thomas N. (University Park, PA), et Al.
Assignee: The Trustees of Pennsylvania State University (University Park, PA)
Application No.: 09/449,559 filed November 29,1999
Patent Pending

"An All-Organic Integrated Emissive Pixel"
Inventors: Jackson, Thomas N. (Univeristy Park, PA), et Al.
Assignee: The Trustees of Pennsylvania State University (University Park, PA)
Application No.: 60/125,665 filed March 22,1999
Abandoned.

"Organic Light Emitters with Improved Carrier Injection"
Inventors: Jackson, Thomas N. (University Park, PA), et Al.
Assignee: The Trustees of Pennsylvania State University (University Park, PA)
Application No.: 60/141,161 filed June 25,1999
US Patent 9,602,438

"Aqueous-Based Photolithography on Organic Materials"
Inventors: Jackson, Thomas N. (University Park, PA), et Al.
Assignee: The Trustees of Pennsylvania State University (University Park, PA)
Application No.: 60/212,189 filed June 16,2000
Patent Pending.

APPENDIX B.
BOOK CHAPTERS AND TECHNICAL REPORTS
(related to this DARPA-sponsored program)

Princeton (Wagner and Sturm Groups) Book Chapters

"Novel Process Technology for Macroelectronics," S. Wagner, H. Gleskova, J.C. Sturm, and Z. Suo, in *Technology and Applications of Hydrogenated Amorphous Silicon*, R.A. Street, ed., pp. 222-251, (Springer, Berlin) 2000.

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APPENDIX C.
JOURNAL AND PROCEEDING PUBLICATIONS
(related to this DARPA-sponsored program)

Fonash Group Papers

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T. N. Jackson, "Pentacene Organic Thin Film Transistors for Large Area Electronics Applications," *SPIE 46th Annual Meeting, Conference 4466*, (July 2001). Invited talk.

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J.A. Nichols, D. J. Gundlach, and T. N. Jackson, "Potential Imaging of Pentacene Organic Thin Film Transistors," 43nd Electronic Materials Conference Digest (June 2001).

D. J. Gundlach, J. A. Nichols, L. Zhou, and T. N. Jackson, "Napthacene Thin Film Transistors," 43nd Electronic Materials Conference Digest (June 2001).

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T. N. Jackson, "Organic Thin Film Transistors for Large Area Electronics Applications," *2001 Electron, Ion, and Photon Beam Technology, and Nanofabrication*, (June 2001). Invited talk.
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T. N. Jackson, "Organic Thin Film Transistors," Pacifichem2000, Honolulu, Hawaii (December 2000). Invited talk.

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T. N. Jackson C. D. Sheray, J. A. Nichols, J. R. Huang, D. J. Gundlach, H. Klauk, and M. G. Kane, "Organic Thin Film Transistors for Flexible-Substrate Displays," 20th International Display Research Conference (IDRC), (September 2000). Invited talk.

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T. N. Jackson, "Pentacene Organic Thin Film Transistors," 42nd Electronic Materials Conference Digest, p. 24 (June 2000). Invited talk.

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T. N. Jackson, "Organic Thin Film Transistors," 2000 American Physical Society Meeting Digest (March 2000). Invited talk.

C. D. Sheraw, D. J. Gundlach, and T. N. Jackson, "Spin-On Polymer Gate Dielectric for High Performance Organic Thin Film Transistors,"
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1999 Materials Research Society Spring Meeting Digest, p. 61 (April 1999).

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J. Wang, Y. Y. Lin, W. Qian, and T. N. Jackson, "Thin-Film Transistors with High Carrier Mobility based on Solution-Cast Poly(3-Alkyl Thiophene)," 1998 Materials Research Society Fall Meeting Digest, p. 372 (December 1998).

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D. B. Thomasson, M. Bonse, R. J. Koval, J. R. Huang, C. R. Wronski, and T. N. Jackson, "Tri-Layer a-Si:H TFTs on Polymeric Substrates," 56th Device Research Conference Digest, pp. 126-127 (June 1998).

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D. B. Thomasson and T. N. Jackson, "Fully Self-Aligned Tri-Layer a-Si:H Thin Film Transistors with Deposited Doped Contact Layer," IEEE Electron Device Letters, vol. 19, n. 4, pp. 124-126 (April 1998).

T. N. Jackson, Y. Y. Lin, D. J. Gundlach, and H. Klauk, "Organic Thin-Film Transistors for Organic Light-Emitting Flat-Panel Display Backplanes," IEEE Journal of Selected Topics in Quantum Electronics, vol. 4, n. 1, pp. 100-104 (January / February 1998).

APPENDIX D.
PRESENTATIONS
(related to this DARPA-sponsored program)

Fonash Group Presentations

Anand T. Krishnan, Sanghoon Bae, and Stephen J. Fonash, "Fabrication of Microcrystalline silicon TFTs Using an Electron Cyclotron Resonance Plasma Approach", Electrochemical Society Meeting (Fall 2000).

Youngchul Lee, Sanghoon Bae, and Stephen J. Fonash, " A Novel Fabrication Technology for Si TFTs on Flexible Substrates", Electrochemical Society Meeting (Fall 2000).

Sanghoon Bae, Youngchul Lee, Anand T. Krishnan, and Stephen J. Fonash, " Metal-induced Solid Phase Crystallization of a-Si Films on Plastic Substrates", Electrochemical Society Meeting (Fall 2000).

Handong Li, A. Kaan Kalkan, and Stephen J. Fonash, " A High-speed High-sensitivity Si Thin Film Humidity Sensor Deposited by PECVD", Electrochemical Society Meeting (Fall 2000).

Xin Lin[1] and Stephen J. Fonash, "Low Temperature Silicon Dioxide Thin Films Deposited Using Tetramethylsilane for Stress Control and Coverage Applications"
Fall MRS meeting (November 2001).

Wagner Group Presentations

Research associates and students gave or presented most of the talks and posters given or presented under this program. These usually were associated with conference papers listed in APPENDIX C.

1998.
Thirteen talks and three posters were presented by group members.
In addition, S. Wagner gave the following talks related to the present program:
-Printable electronics, University of Linz, Semiconductor Physics Dept., June 17.
-Digital paint, Engineering freshmen, October 11.
-Technology for ultralight, large-area display backplanes, POEM Annual Review, Nov. 4.
-Amorphous silicon transistors on ultrathin steel foil substrates, ECS Symposium on Thin-Film Transistor Technology, Boston, Nov. 4.

1999.
Sixteen talks and three posters were presented by group members.
In addition, S. Wagner gave talks/seminars on:
-Mechanics of film-on-foil electronics, University of Linz, Semiconductor Physics Dept., Jun 21.
-Directly deposited microcrystalline silicon, Workshop on Crystalline Silicon Solar Cell Material and Processes, Breckenridge, CO, August 11, 1999.

2000.
Fourteen talks and two posters given by group members.
In addition, S. Wagner gave talks/seminars related to this program on:
- Large Area Printing for Intelligent Electronic Surfaces, POEM Workshop on Large Area Electronics and Multimedia Systems Interface, 2/15.
- Device Performance under Mechanical Stress, DARPA Information Science and Technology Panel Meeting on Computational Fabrics - Technology, Raleigh, NC, 4/14.
- Large-area flexible electronics, Princeton Materials Institute, 4/19.
- High Resolution Copper Lines by Direct Imprinting, Materials Research Society Spring Meeting, San Francisco, 4/25.
- Thin film transistors on flexible substrates, Materials Research Society Spring Meeting, San Francisco, 4/27.
- Flexible large-area electronics, Instituto Superior Técnico, Lisbon, Portugal, 5/23.
- Integrating Electronics With Textiles, DARPA Information Science and Technology Panel Meeting on Computational Fabrics - Technology, Raleigh, NC, 6/17.
- Nanokristallines Silizium, Abscheidung, Eigenschaften und Anwendungen, University of Linz, Austria, 7/24.

- Low temperature amorphous and nanocrystalline silicon technology for flat panel displays, International Display Research Conference, Palm Beach, Florida, 9/26.
- Polycrystalline silicon thin film transistors, Polyse 2000, St. Malo, France, 9/4.
- Mechanical properties and thin film transistor performance for flexible displays, American Vacuum Society 47th International Symposium, Boston, 10/2.
- Power fiber concepts: Photovoltaic energy harvesting, Defense Science Research Council, 1st Electrotextiles Workshop, Raleigh, NC,10/6.
- Flexible transistor backplanes, Defense Science Research Council Electrotextiles Workshop II, Natick, MA. 12/1.

2001.
Twelve talks and three posters given by group members.
S. Wagner gave talks on:
- Direct Printing of Smart Electronics Surfaces
POEM Technology Venture Workshop, Princeton,1/5.
- Direct printing applied to silicon devices,
Materials Research Society Spring Meeting, 4/20.
- Polycrystalline Silicon on Steel Substrates: Material, Thin-Film Transistors, Integrated Circuits, University of Linz, Institute for Semiconductor Physics, 8/6.
- CMOS polycrystalline silicon circuits on steel substrates
Internat. Conf. Amorphous and Microcrystalline Semiconductors, Nice, France, 8/30.
- Trends in low-cost electronics,
IEEE EDS short course on Future Trends in Microelectronics, Guadalajara, Mexico, 11/17.
- Talks at DARPA workshops and review meetings: 1/31, (e-textiles), 1/16, 5/22, 11/30 (High definition systems)

Sturm Group Presentations

M.H. Lu, E. Ma, J.C. Sturm, and S. Wagner, "Amporphous silicon TFT active-matrix OLED pixel," Meeting LEOS, Orlando, FL (Nov., 1998).

L. Montès, L. Tsebeskov, P.M. Fauchet, K. Pangal, J.C. Sturm, S. Wagner, "Optical analysis of plasma enhanced crystallization of amorphous silicon films", Symp. Mat. Res. Soc., Boston, MA (Nov., 1998).

T.R. Hebner and J.C. Sturm, "Three-color tuning of polymer luminescence color by local dye droplet application," Symp. Mat. Res. Soc., Boston, MA (Nov., 1998).

K. Pangal, J.C. Sturm, and S. Wagner, "Hydrogen plasma-enhanced crystallization of amorphous silicon for low-temperature polycrystalline silicon TFT's," *Tech. Dig. Int. Elec. Dev. Mtg.* 261-264 (1998).

K. Pangal, Y. Chen, J.C. Sturm, S. Wagner, "Integrated amorphous and polycrystalline silicon TFTs with a single silicon layer", Symp. Mat. Res. Soc., San Francisco, CA (April, 1999).

X. Jiang, R.A. Register, F. Pschenitzka, and J.C. Sturm, "Doped organic light-emitting diodes based on random copolymer containing both hole and electron transport groups," Symp. Mat. Res. Soc., San Francisco, CA (April, 1999).

F. Pschenitzka and J.C. Sturm, "Three-color doping of polymer OLED's by masked dye diffusion," Symp. Mat. Res. Soc., San Francisco, CA (April, 1999).

(Invited) J.C. Sturm, T.R. Hebner, F. Pschenitzka, and M.H. Lu, "System constraints and printing for large-area organic light-emitting displays," Proc. Asia-Pacific Symp. on Organic Electroluminescent Materials and Devices, Hong Kong, China (June, 1999).

Y. Chen, K. Pangal, J.C. Sturm and S. Wagner, "P-channel thin film transistor of microcrystalline silicon directly deposited at 320 °C," IEEE Dev. Res. Conf., Santa Barbara, CA (June, 1999).

(Invited) J.C. Sturm, F. Pschenitzka, T.R. Hebner, M.HY. Lu, and S. Troian, "Printing approaches for large-area color organic LED displays," SPIE, Denver, CO (July, 1999).

Y. Chen, K. Pangal, J.C. Sturm, and S. Wagner, "P-channel microcrystalline silicon thin film transistor fabricated at 320 °C," 18th Int. Conf. Amorph. and Microcryst. Silicon," Snowbird, UT (Aug. 1999).

M. Wu, Y. Chen, K. Pangal, J.C. Sturm, and S. Wagner, "High-performance polysilicon thin film transistors on steel substrates," 18th Int. Conf. on Amorphous and Microcrystalline Semiconductors, Snowbird, UT (Aug. 1999).

(Invited) J.C. Sturm, F. Pschenitzka, T.R. Hebner, M.H. Lu, and S. Troian, "Large-Area Printing Technologies for Full Color OLED Integration," Organic Light Emitting Materials-99, Frontier Science Research Conf, La Jolla, CA (Nov. 1999).

M. Wu, K. Pangal, J.C. Sturm and S. Wagner, "High temperature polycrystalline silicon thin film transistor on steel substrates," Tech. Dig. Int. Elec. Dev. Mtg., Washington, DC (Dec. 1999).

(Invited) J.C. Sturm, F. Pschenitzka, T.R. Hebner, M.H. Lu, B. Diamond, and S. Troian, " Fundamental and practical issues in large-area polymer pattering for polymer LED displays," Symp. Mat. Res. Soc., San Francisco, CA (April, 2000).

M.H. Lu, C.F. Madigan, and J.C. Sturm, "Experiment and modeling of conversion of substrate waveguided modes to surface emitted light by substrate patterning," Symp. Mat. Res. Soc., San Francisco, CA (April, 2000).

F. Pschenitzka and J.C. Sturm, "Photolithographically patterned dye diffusion into organic thin-films for OLED application using soft masks," Symp. Mat. Res. Soc., San Francisco, CA (April, 2000).

" C. Madigan, B. Diamond, T.R. Hebner, F. Pschenitzka, X. Jiang, R. Register, S. Troian, and J.C. Sturm, Lateral redistribution and film profiles during ink-jet printing of polymer LED's, Symp. Mat. Res. Soc., San Francisco, CA (April, 2000).

F. Pschenitzka, C. Madigan, M.H. Lu, and J.C. Sturm, "Patterning technology for polymer OLED displays," SPIE Symp., San Diego, CA (July, 2000).

M.H. Lu, C.F. Madigan, and J.C. Sturm, "Improved external coupling efficiency in organic light-emitting devices on high-index substrates," Tech. Dig. Int. Elec. Dev. Mtg., San Francisco, CA (Dec, 2000).

F. Pschenitzka, and J.S. Sturm, "Photographically patterned dye diffusion into organic thin films for OLED applications using soft masks," presented at Mat Res. Soc, San Francisco, CA (April, 2000).

F. Pschenitzka and J.C. Sturm, "Patterned dye diffusion using transferred photoresist for Polymer OLED displays, SPIE (2000).

F. Pschenitzka and J.C. Sturm, "Patterning of OLED Cathodes by Metal Dry-Etching, SID Int. Symp. Soc. Inf. Dips. (2001).

K. Long, M.-H. Lu, F. Pschenitzka and J.C. Sturm, "Novel-three-color polymer light-emitting devices for passive matrix flat panel displays," 59th Dev. Res. Conf, South Bend, IN (June, 2001).

(Invited) M.H. Lu and J.C. Sturm, "Output coupling in organic light-emitting devices: modeling and experiments, Symp. SPIE, San Diego (July, 2001).

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T. N. Jackson, "Pentacene Organic Thin Film Transistors for Large Area Electronics Applications," *SPIE 46th Annual Meeting, Conference 4466*, (July 2001). Invited talk.
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J. R. Huang, W. Qian, H. Klauk, T. N. Jackson, K. Black, P. Deines-Jones, and S. D. Hunter, "Active-Matrix Pixelized Well Detectors on Polymeric Substrates," *51st National Aerospace and Electronics Conference Digest* (October 2000).

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T. N. Jackson, "Pentacene Organic Thin Film Transistors," *42nd Electronic Materials Conference Digest*, p. 24 (June 2000). Invited talk.

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D. J. Gundlach, C. D. Sheraw, H. Klauk, J. A. Nichols, J. R. Huang, and T. N. Jackson, "Photolithographically Defined Pentacene Thin Film Transistors on Flexible Plastic Substrates," *46th International Symposium of the American Vacuum Society Technical Program*, p. 85 (October 1999).

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APPENDIX E.
GRADUATE DEGREES GRANTED AND RESEARCHERS TRAINED
(related to this DARPA-sponsored program)

Pennsylvania State University (Fonash and Jackson Groups)

Fonash Group

Ph.D. Candidates: Daniel Hayes, Joseph Cuiffi, Handong Li, Kyuhwan Chang

Ph.D Degrees Awarded: Xin Lin, Ali Kaan Kalkan, Hong Zhu, Anand Krishnan

Jackson Group

Ph.D. Degrees Awarded: Dave Gundlach, Jeffrey Huang, Hagen Klauk

Master of Science in Electrical Engineering (MSEE) Degrees Awarded:
Mathias Bonse, Chris Baiocco

Post-Doctoral Researchers: Jianna Wang

Princeton University (Wagner and Sturm Groups)

Wagner Group

Ph.D. Degrees Awarded:
Adam Payne, Brian Crone, Yu Chen, Eugene Ma, Cheong-Min Hong, Ming Wu

Sturm Group

Co-investigator: Prof. James C. Sturm, Department of Electrical Engineering, Director: Center for Photonics and Optoelectronic Materials, Princeton University, Princeton NJ: partial academic year and summer support.

Ph.D Candidates: Michael Min-Hao Lu, Florian Pschenitzka

Ph.D. Degree Awarded: Kiran Pangal

Master of Science in Engineering (MSE) Degrees Awarded:
Thomas Hebner, Lori Stirling

Bachelor of Science in Engineering (BSE) Degree Awarded:
Conor Madigan

LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

AFRL	Air Force Research Laboratory
Ag	Silver
Alq3	Aluminum tri-quinolate (electron transporting material)
AMLCD	Active matrix liquid crystal display
AMOLED	Active matrix organic light emitting diode (display)
a-Si	Amorphous silicon
a-Si:H	Amorphous silicon passivated with hydrogen
p-Si	Polycrystalline silicon, also know as poly-silicon
μ-Si, n-Si	Microcrystalline silicon, also known as nanocrystalline silicon
ε	Dielectric constant, or mechanical strain
σ	Electrical conductivity, or mechanical stress
λ	Wavelength
η	Compressive strain
μ	Mobility
Ω	Ohm
μm	Micrometer
Å	Ångstrøm
A	Area
$A \cdot cm^{-2}$	Amperes per square centimeter, a unit of electrical current density
AISI	American Iron and Steel Institute
Al	Aluminum
a-Si	Amorphous silicon
a-Si:H	Hydrogenated amorphous silicon
ASIC	Application-specific integrated circuits
AZ5214	A type of photoresist
BOE	Buffered oxide etch
C6	Coumarin 6 (a dye)
cc	Cubic centimeter
CCl_2F_2	Carbon dichloride difluoride, a plasma etchant
cm^{-1}	Reciprocal centimeters, a measure of wavenumber
cm^2/Vs	Unit of electron of hole mobility
CMOS	Complementary Metal Oxide Silicon
Cr	Chromium
C_{SiN}	Capacitance of the gate insulator
d	Thickness
DARPA	Defense Advanced Research Projects Agency
E_0	Urbach energy
E_g	Energy band gap of a semiconductor
eV	Electron Volt
ECR	Electron cyclotron resonance
EL	Electroluminescence
FPD	Flat panel display
FT-IR	Fourier Transform InfraRed
GPa	Gigapascal (10^9 Pa)

H_2	Hydrogen
H_2O_2	Hydrogen peroxide
H_2SO_4	Sulfuric acid
HDS	High Definition Systems
HPD	
HOMO	Highest Occupied molecular orbital
i	Not intentionally doped (as in "*i* nc-Si")
IC	Integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
II-VI	Stoichiometric compound made of one element of column II and another of column VI of the periodic table
I_{leak}	Gate leakage current
I_{off}	Off-current
I_{on}	On-current
IJP	Ink jet printing
ITO	Indium tin oxide (thin film)
IP	Intellectual property
K	Output voltage gain $K = \Delta V_{OUT}/\Delta V_{IN}$
L	Channel length
L	Liter
LCD	Liquid crystal display
LUMO	Lowest unoccupied molecular orbital
MEMS	Micro-electro-mechanical systems
MHz	Megahertz
MILC	Metal induced crystallization
MOSFET	Metal-oxide-semiconductor field-effect transistors
Mtorr	Millitorr (10^{-3} torr, about 0.134 Pa)
MV/cm	Megavolt per centimeter, a measure of electric field strength
n	Index of refraction (ratio of speed of light in vacuum to a specified medium)
n^+	"n-plus," a symbol for high n-type dopant concentration
n^+	Highly n doped (as in "n^+ nc-Si")
N_2	Nitrogen
nc-Si	Nanocrystalline silicon
n-channel	Transistor with negative doping in conduction channel connecting source to drain
n-TFT	n-channel thin-film-transistor
NH_3	Ammonia
nit	Candela per meter^2 (standard unit of luminance)
nm	Nanometer
O_2	Oxygen
OLED	Organic light emitting diode
OTFT	Organic thin-film transistor
P	Pressurel
p^+	Highly p doped (as in "p^+ nc-Si")
Pa	Pascal (a measure of force per unit area)
p-channel	Transistor with positive doping in conduction channel connecting source to drain
p-TFT	p-channel thin-film-transistor

PBD	2-(4-biphenylyl)-5-(4-*tert*-butyl-phenyl)-1,3,4-oxadiazole
PC	Polycarbonate (an engineering plastic)
PECVD	Plasma enhanced chemical vapor deposition
PH_3	Phosphine
PL	Photoluminescence
Poly-Si	Polycrystalline silicon
Polysilicon	Polycrystalline silicon
PVK	Poly(N-vinyl carbazole), a hole-transporting polymer
QMMM	Quantum Mechanical Microcavity Model
R	Hydrogen-dilution ratio, or bending radius
RBS	Rutherford back-scattering spectrometry
RF	Radio frequency
RGB	Red, Green, Blue
RH	Relative humidity
RIE	Reactive ion etching
RMS	Root mean square
S	Subthreshold slope, $S \equiv d(V_{gs})/d(\log_{10}I_d)$
Si	Silicon
$S \cdot cm^{-1}$	Siemens per centimeter, unit of electrical conductivity
s.s. or SS	Stainless steel
S/D	Source/Drain
sccm	Standard cubic centimeters per minute
Si	Silicon
$SiCl_2H_2$	Dichlorosilane
SiF_4	Silicon tetrafluoride
SiH_4	Silane
SIMS	Secondary ion mass spectrometry
SiN_x	Silicon nitride
SiO_2	Silicon dioxide
SOG	Spin On Glass
SID	Society for Information Display
SPC	Solid phase crystallization
SPIE	International Society for Optical Engineering
T_f	Falltime
TFT	Thin film transistor
Ti	Titanium
TMS	Tetramethylsilane
t_{ox}	Oxide thickness
T_r	Rise time
UV	Ultraviolet
µL	Microliter (10^{-6} liter)
V_{DD}	Supply voltage
V	Volt
V_{th}	Threshold voltage
W	Channel width
Y	Modulus of elasticity

GLOSSARY

Amorphous (as in amorphous silicon).

Polycrystalline (as in "poly"crystalline silicon).

Microcrystalline (as in "micro"crystalline silicon).

Nanocrystalline (as in "nano"crystalline silicon).

304 stainless steel: An alloy of Fe/Cr/Ni at 72/18/10 wt.%

Backplane: The substrate and addressing electronics of a display

Compound semiconductors: Semiconductors made of several chemical elements, as in GaAs or CdTe.

Corning 7059: A glass made by Corning.

Dektak: Manufacturer of stylus surface profilers

Die of a mask set: Unit of a mask set whose replication covers an entire wafer with identical circuits.

Dopant: Impurity added to a semiconductor to modify its electrical conductivity.

Electron-cyclotron-resonance: Technique for exciting a glow discharge in a reactant gas.

Ellipsometry: Measurement of the degree of polarization of light, used for determining thickness and refractive index of transparent thin films.

Frontplane: The light modulating or emitting portion of a display, including encapsulation

Kapton E: A polyimide made by Dupont.

Microblock: Very small silicon integrated circuits, typically a few hundred micrometers on a side. Also called nanoblocks.

Mobility: In solids, the proportionality factor between electron velocity and electric field.

Modulus of elasticity: Proportionality factor between mechanical stress and strain.

Neutral plane: Surface within a solid that is free of strain.

Passivation: Rendering inert against an undesired action, e.g., corrosion, breakage.

Poisson ratio: Term describing the ratio between strain perpendicular to the applied mechanical stress, and strain parallel to the applied stress.

Polyimide: A goup of organic polymers characterized by the imide linkage –CONCO- .

Pull-up, pull-down devices: Components of logic circuits.

Raman scattering: Technique for determining crystallinity of thin films.

Reactive ion etching: A technique where ions made in a glow discharge erode the surface of a solid.

Rutherford back-scattering: A technique in which high velocity ions are bounced off a solid. Used to obtain formation on the chemical composition of the solid. Secondary ion mass spectrometry: A technique in which an ion beam (of typically cesium or oxygen) knocks loose ions from the surface of a solid. These secondary ions are analyzed by mass spectrometry to obtain information on the composition of the solid.

Threshold voltage: The voltage at which a electron device, specifically a field effect transistor, turns on.

X-ray diffraction: Technique for determining crystallinity.

Young's modulus: Proportionality factor between mechanical stress and strain.

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